APPLICATION NOTE

RELEASED 1/23/18

Power-up Sequencing UT54LVDS217/218

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number
3.3V Serializer	UT54LVDS217	5962-01534	01, 02	WD11, WD13
3.3V Deserializer	UT54LVDS218	5962-01535	01, 02	WD12, WD14

1.0 Overview

Field applications of the UT54LVDS217 and UT54LVDS218 devices are often times physically separate distributed systems that are controlled and powered-up individually and autonomously, requiring in turn non-simultaneous power-up sequencing of the UT54LVDS217 and UT54LVDS218 devices. In order to meet the needs of customers who deploy applications of systems of the aforementioned distributed architecture, CAES Semiconductor Solutions performed a design-based simulation analysis of the UT54LVDS217/218 products to characterize the functional behavior of these devices, when operated in systems requiring non-simultaneous power-up sequencing and startup. The design simulations involved six separate scenarios for the power-up sequencing, each of which was simulated for the minimum and maximum specified input clock frequencies and three Process, Voltage and Temperature (PVT) corners, resulting in total of 36 simulation scenarios for each of the UT54LVDS217/218 devices. This application note replaces AN-LVDS-003-01 application note.

Table 2: Summary of Power-up Simulation Scenarios

Test No.	VDD ramp [s]	/pwrdn ramp [s]	T_dly VDD [s]	T_dly /pwrdn [s]	Fclk [MHz]
1	10m	10m	0	0	15
2	100m	100m	0	0	15
3	10m	10n	0	10.1m	15
4	100m	10n	0	100.1m	15
5	10m	10n	100u	0	15
6	100m	10n	100u	0	15
7	10m	10m	0	0	75
8	100m	100m	0	0	75
9	10m	10n	0	10.1m	75
10	100m	10n	0	100.1m	75
11	10m	10n	100u	0	75
12	100m	10n	100u	0	75

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2.0 Power-up Sequence Simulation Scenario Description

Table 2 summarizes the six separate power-up scenarios that were simulated independently on both UT54LVDS217 and UT54LVDS218 devices, for the minimum and maximum specified input clock frequencies of 15MHz and 75MHz respectively, and the Slow, Typical and Fast PVT corners (Slow Corner is Slow Process/T_J=125°C/VDD=3.0V; Typical Corner is Typical Process/T_J=25°C/VDD=3.3V; Fast Corner is Fast Process/T_J=–55°C/VDD=3.6V). As seen in Table 2, the power-up scenarios were modeled as combinations of VDD and /POWERDOWN pin rising ramp waveforms, with three different rise times: 10 milliseconds, 100 milliseconds and 10 nanoseconds, in addition to three separate time delays of the VDD ("T_dly VDD") and the /POWERDOWN ("T_dly /pwrdn") signal start times, relative to time 0 of the start of each simulation scenario. These combinations were intended to capture any possible interdependency between the orders of assertion of the VDD and /POWERDOWN signal and their effect on the ability of the SERDES devices to achieve successful PLL startup and eventual lock. A simulation scenario was considered to pass the test if it resulted in successful PLL startup represented by the appearance of 500 cycles of device output clock, with the correct frequency multiplied from the reference input clock (15MHz or 75MHz) and less than 2 nanoseconds of clock skew internal to the PLL. In all simulation scenarios, it is assumed that the input data and the input clock signals are stable and valid, before the power-up sequence is applied.

Figure 1 illustrates the power-up sequence Test #1 in Table 2. In this scenario, the VDD and the /POWERDOWN pin are ramped-up simultaneously with a ramp duration of 10 milliseconds, while the inputs of the UT54LVDS217/218 devices are presented with valid clock and data signals. Test #2 is performed with identical power-up sequencing as Test #1, but the ramp duration is 100 milliseconds.

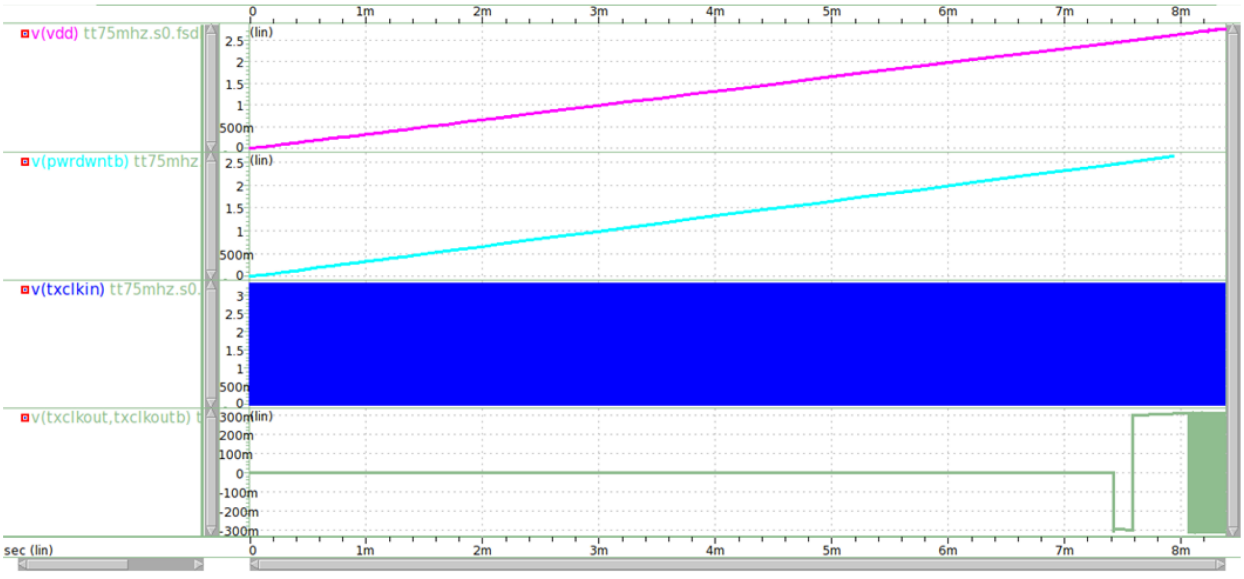

Figure 1: Power-up Scenario Test #1 (Table 2) waveforms

Figure 2 illustrates the Test #3 power-up sequence, in which the VDD is ramped from 0 to full level in 10ms, and /POWERDOWN signal is de-asserted (set to logic HIGH) after 100 microseconds from VDD reaching full level. The /POWERDOWN signal ramp is 10 nanoseconds.

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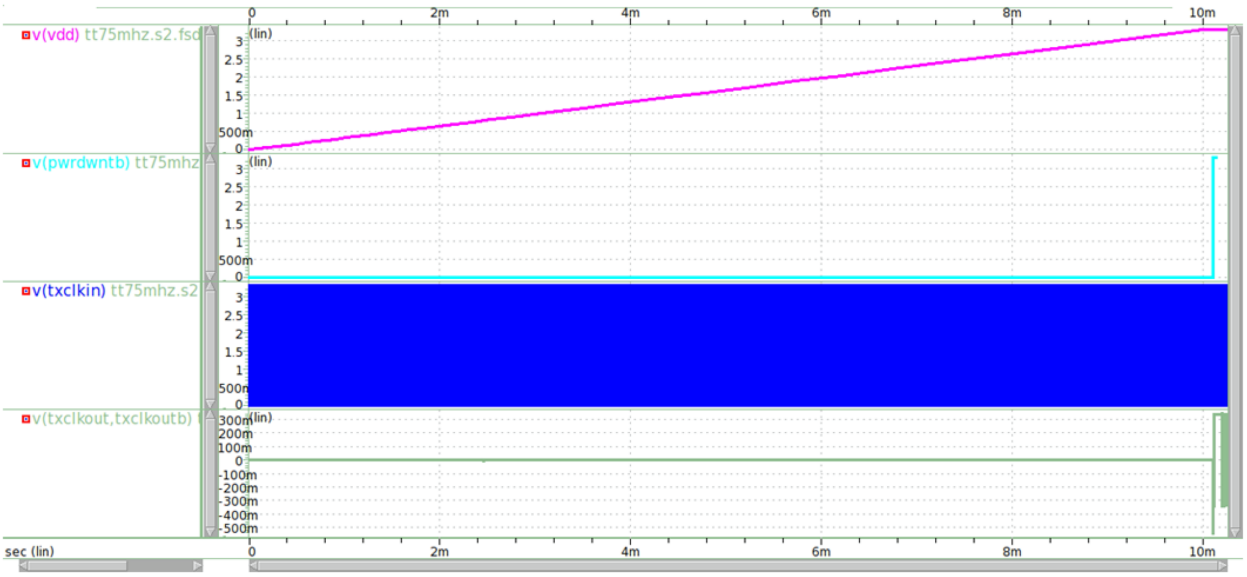

Figure 2: Power-up Scenario Test #3 (Table 2) waveforms

Test #4 power-up sequence is identical to Test #3 with the only difference of the ramp duration being 100 milliseconds and the applied time delay "T_dly/pwrdn" of 100.1 milliseconds, which results in the /POWERDOWN signal being set to logic HIGH, 100 microseconds after VDD has reached full level.

Figure 3 illustrates the Test #5 power-up sequence. As seen in Figure 3, in this test scenario, the /POWERDOWN signal is set to logic HIGH with a ramp duration of 10 nanoseconds, before VDD is ramped to level with a ramp duration of 10 milliseconds. The VDD ramp start is 100 microseconds after /POWERDOWN signal was set to logic HIGH. Test #6 power-up sequence is identical to Test #5 power-up sequence, with the only difference being the VDD ramp duration of 100 milliseconds.

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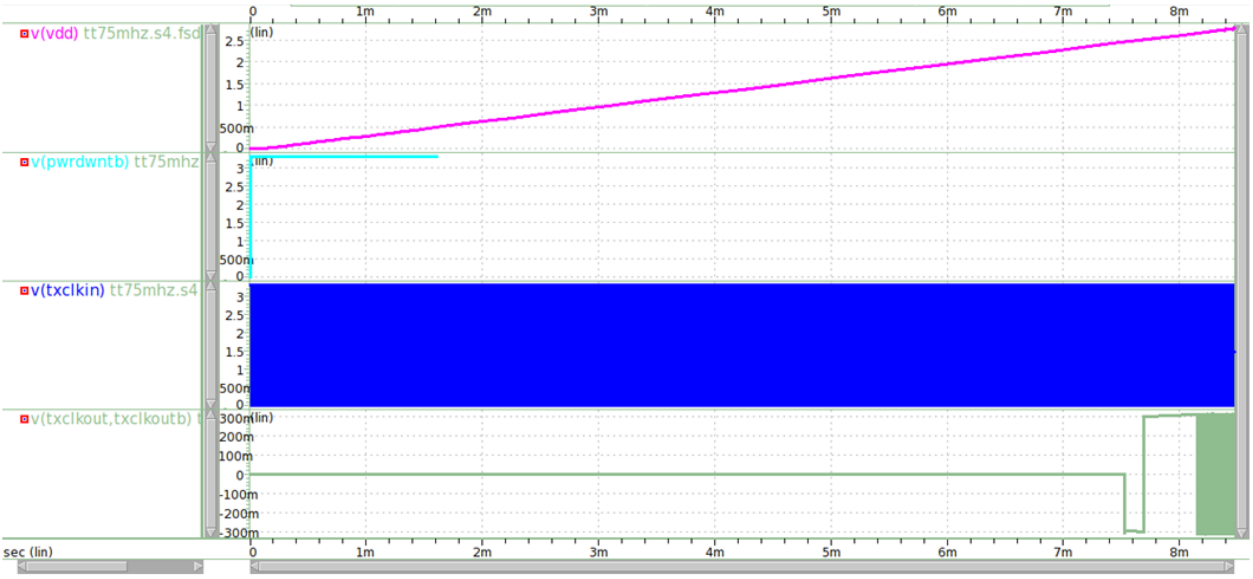

Figure 3: Power-up Scenario Test #5 (Table 2) waveforms

3.0 Power-up Sequence Simulation Results

Table 3 summarizes the UT54LVDS217/218 design simulation results for the various different power-up sequence scenarios and the three separate PVT corners. As seen in Table 3, all simulated power-up scenarios and PVT corners resulted in successful PLL startup.

Table 3: UT54LVDS217/218 Power-up Sequence Simulation Results

	UT54LVDS217 PLL startup time [s] (from time 0)			UT54LVDS218 PLL startup time [s] (from time 0)		
Test No.	**Typical Corner**	**Slow Corner**	**Fast Corner**	**Typical Corner**	**Slow Corner**	**Fast Corner**
1	8.208m	9.359m	7.245m	8.22m	9.36m	7.24m
2	73.2m	81.4m	64.9m	75.38m	86.89m	67.13m
3	10.25m	10.44m	10.193m	10.26m	10.44m	10.19m
4	100.25m	100.44m	100.19m	100.25m	100.44m	100.19m
5	8.315m	9.466m	7.337m	8.31m	9.46m	7.34m
6	73.3m	81.5m	65m	75.45m	86.98m	67.26m
7	8.373m	9.60m	7.313m	8.362m	9.582m	7.318m
8	76.08m	87.45m	67.21m	75.84m	87.45m	67.44m
9	10.25m	10.57m	10.15m	10.24m	10.56m	10.15m
10	100.25m	100.56m	100.15m	100.25m	100.56m	100.15m
11	8.463m	9.69m	7.410m	8.445m	9.682m	7.418m
12	76.17m	87.55m	67.32m	75.97m	87.54m	67.54m

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3.1 Power-up Sequence Measurement Results

In order to perform design simulation result verification, a selected number of power-up sequence scenarios was experimentally measured in the lab, using the UT54LVDS217/218 evaluation board, a sample of each of UT54LVDS217/218 SERDES devices and appropriate test and measurement equipment comprised of a power supply, pulse generator and oscilloscope for generating and capturing the corresponding signal waveforms. Table 4, summarizes the measurement result for the power-up sequence scenarios Test #1 through Test #6 (15MHz input clock frequency), for each of UT54LVDS217/218 sample devices at the Typical PVT corner. As seen in Table 4, there exists a very good correlation between the simulated and measured results of the selected power-up sequence test scenarios at the Typical PVT corner. Appendix A – UT54LVDS217/218 Typical PVT Corner Measured Waveforms, provides a complete overview of the oscilloscope-captured measurement result waveforms.

Table 4: UT54LVDS217/218 Typical PVT Corner Measurement Results

	UT54LVDS217 PLL startup time [s] (from time 0)		UT54LVDS218 PLL startup time [s] (from time 0)	
Test No.	Typical Corner Simulated	Typical Corner Measured	Typical Corner Simulated	Typical Corner Measured
1	8.208m	9.32m	8.22m	8.0m
2	73.2m	77.2m	75.38m	72.8m
3	10.25m	10.28m	10.26m	10.2m
4	100.25m	100.8m	100.25m	101.6m
5	8.315m	8.56m	8.31m	7.96m
6	73.3m	78.8m	75.45m	74.4m

4.0 Summary and Conclusions

Based on the results obtained from the design simulations of all the different power-up scenarios and simulated PVT corners, we conclude that the UT54LVDS217/218 devices are not sensitive to any particular sequence of application of the VDD power supply and the /POWERDOWN control signal ramps and that they start functioning properly, as soon as the device PLL completes its startup process during the power-up sequence of choice. The VDD power and the /POWERDOWN signal ramps can be applied in any order, with the only requirement that the device inputs are presented with valid input clock and data signals, before the device PLL begins the startup process. It is to be noted that if a valid clock is not present at the clock input of each device when the PLL is enabled during the power-up sequence, a possibility exists that the PLL could begin to lock to a periodic noisecoming from the system environment. We therefore recommend that system designers provide for the ability to independently control the /POWERDOWN pin on each device, to enable clean PLL startup and re-lock once the correct input clock with the correct frequency is establish at the device clock input pins.

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Appendix A – UT54LVDS217/218 Typical PVT Corner Measured Waveforms

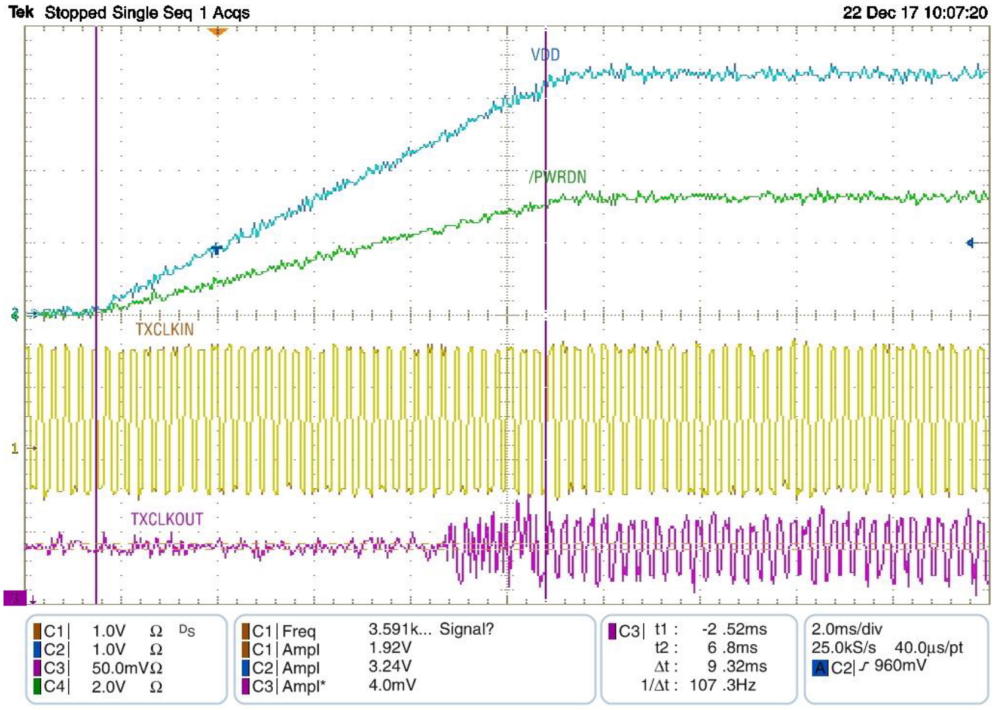

Figure 4: UT54LVDS217 Test #1 Typical PVT Corner Measured Waveform

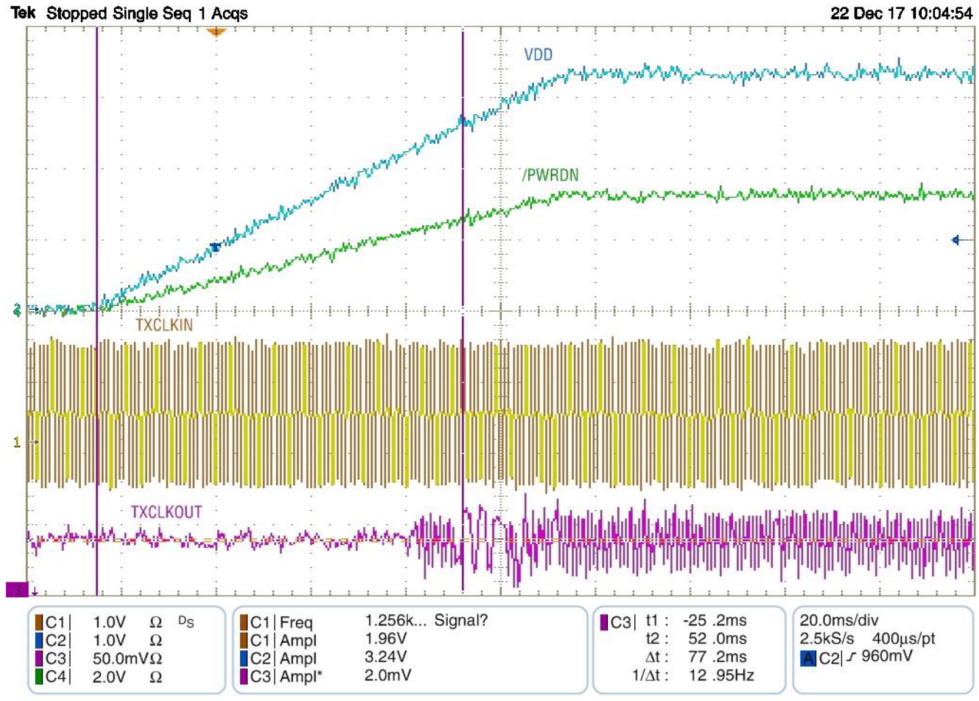

Figure 5: UT54LVDS217 Test #2 Typical PVT Corner Measured Waveform

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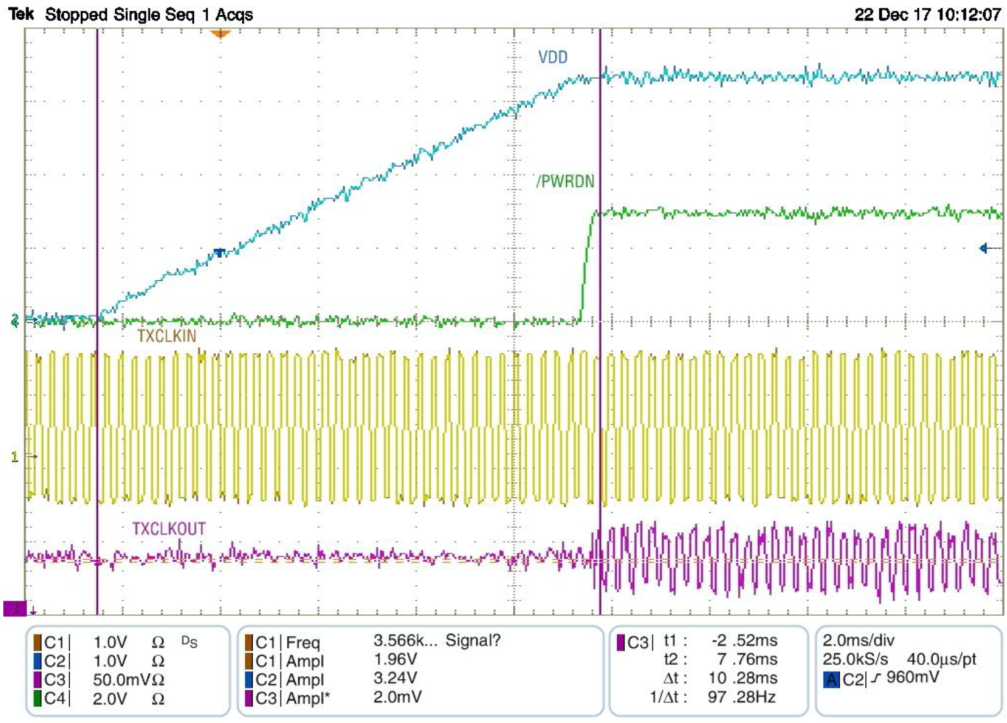

Figure 6: UT54LVDS217 Test #3 Typical PVT Corner Measured Waveform

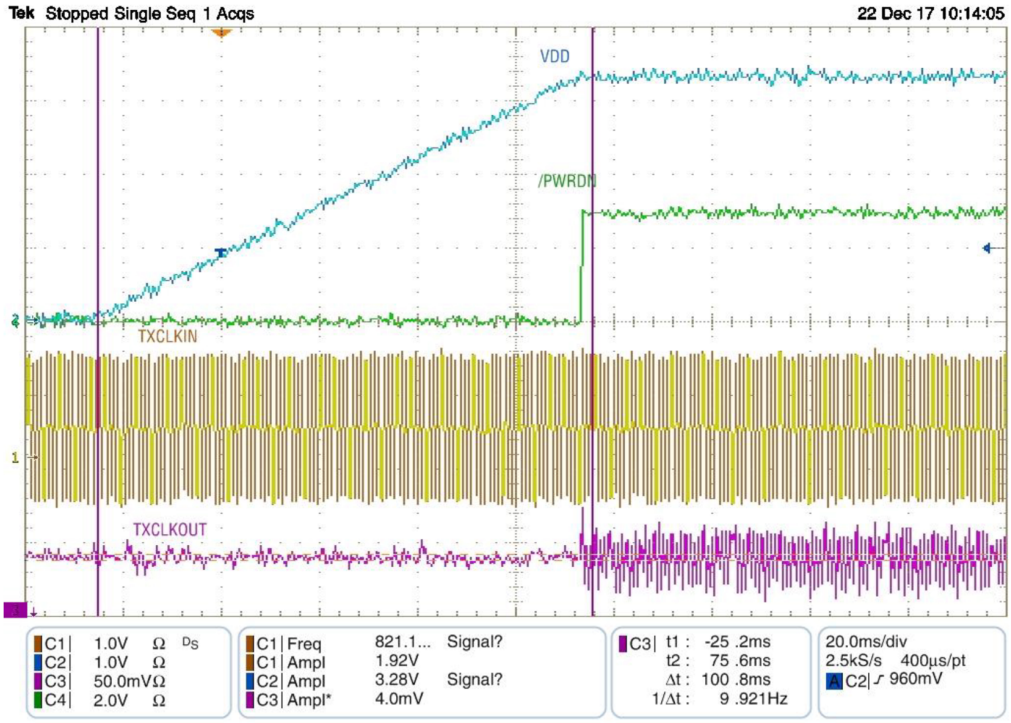

Figure 7: UT54LVDS217 Test #4 Typical PVT Corner Measured Waveform

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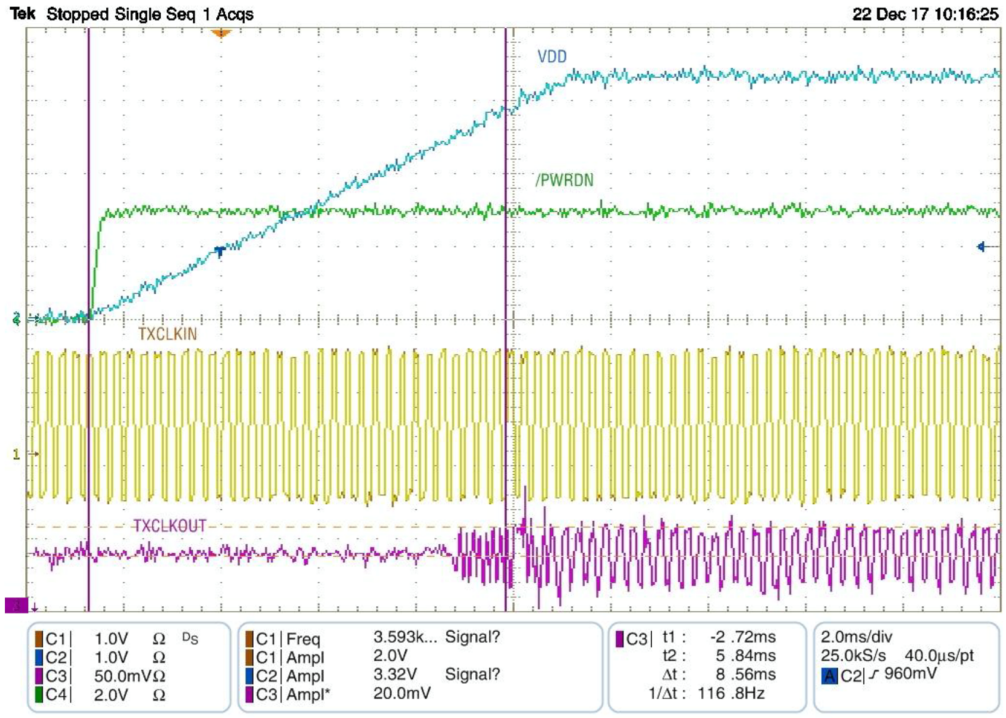

Figure 8: UT54LVDS217 Test #5 Typical PVT Corner Measured Waveform

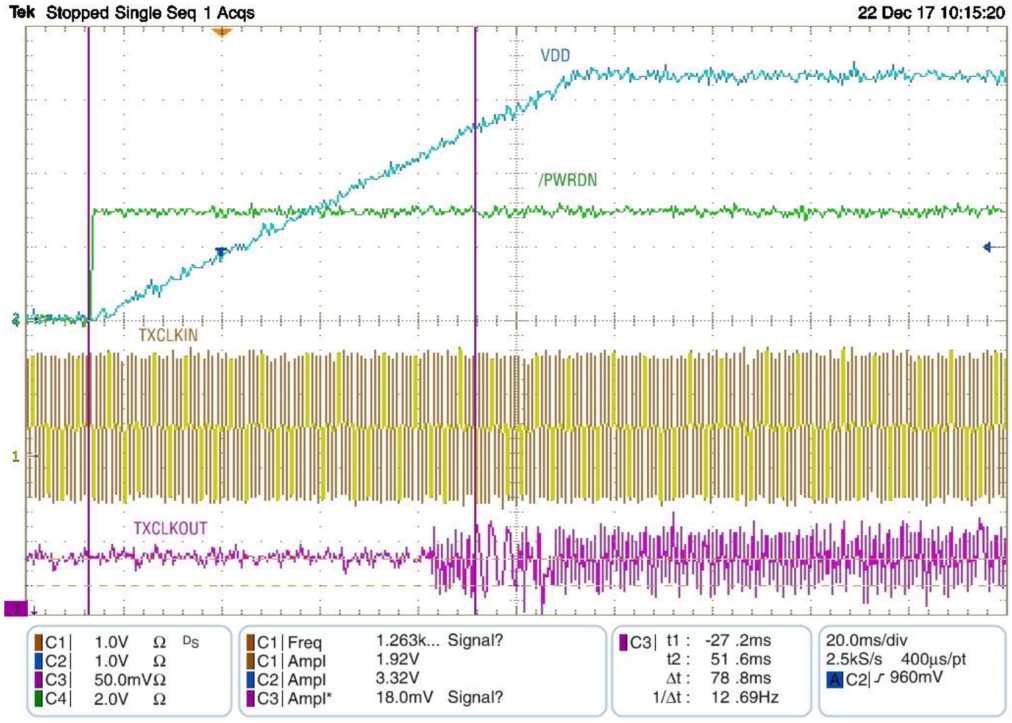

Figure 9: UT54LVDS217 Test #6 Typical PVT Corner Measured Waveform

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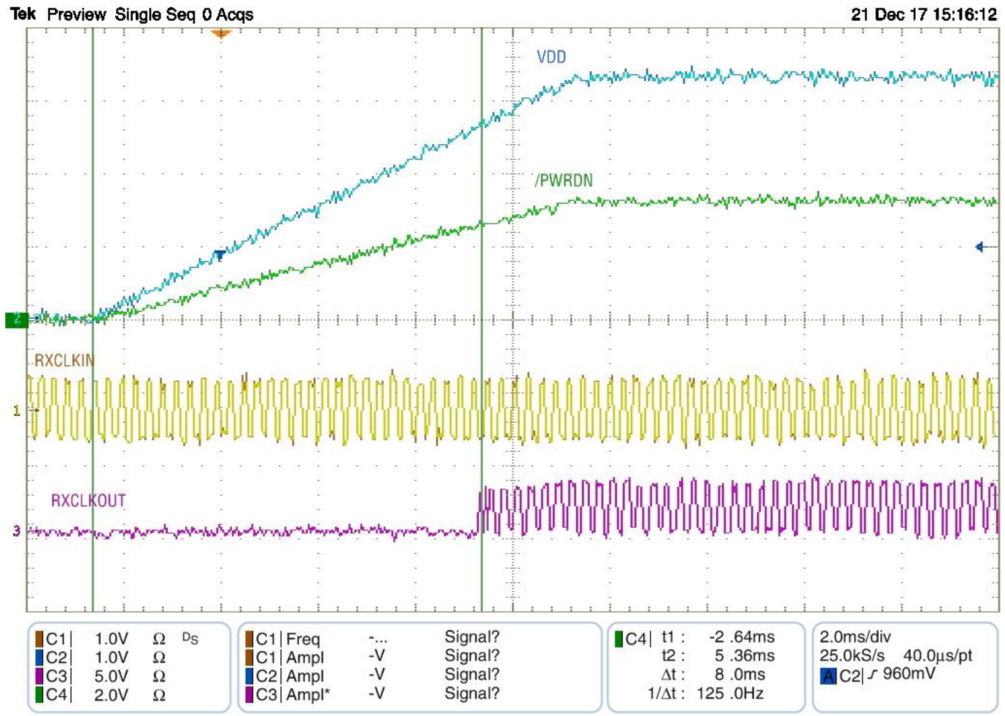

Figure 10: UT54LVDS218 Test #1 Typical PVT Corner Measured Waveform

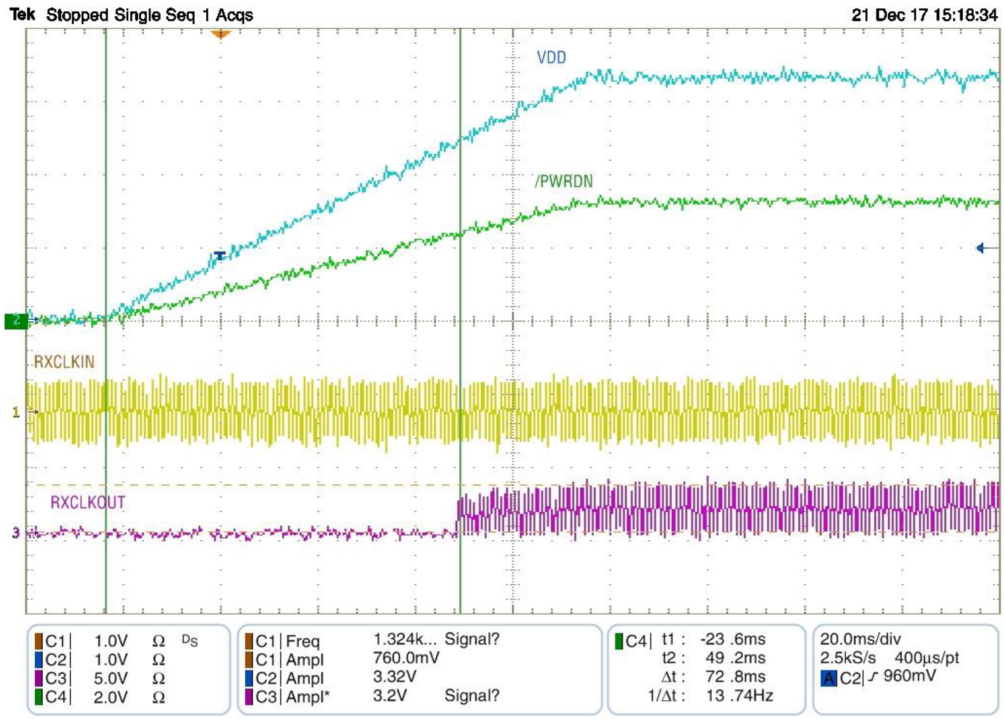

Figure 11: UT54LVDS218 Test #2 Typical PVT Corner Measured Waveform

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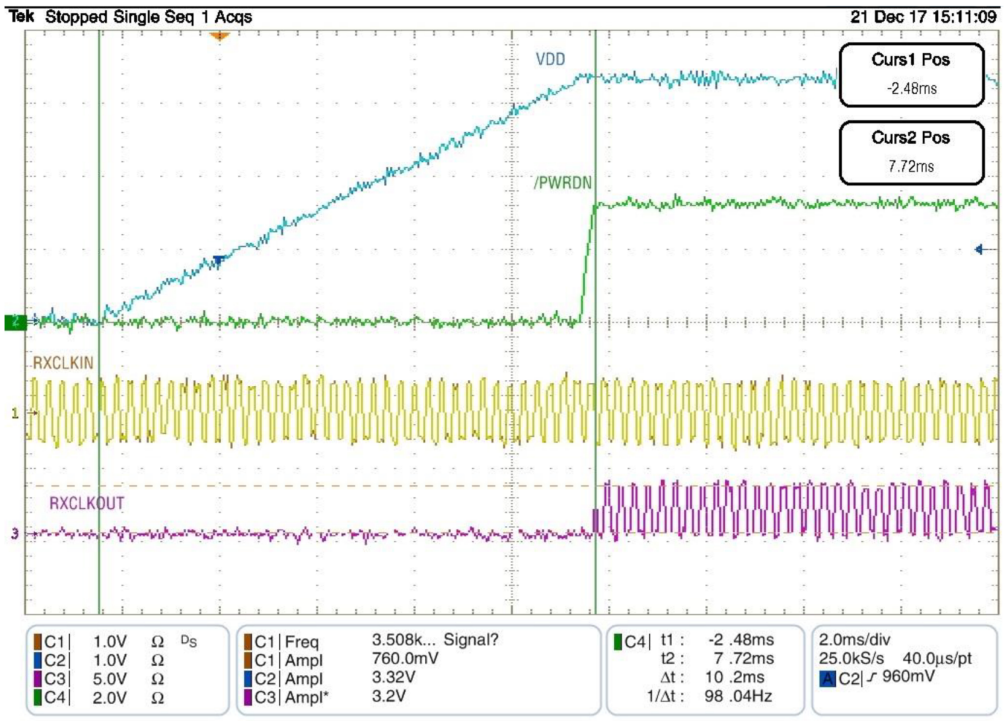

Figure 12: UT54LVDS218 Test #3 Typical PVT Corner Measured Waveform

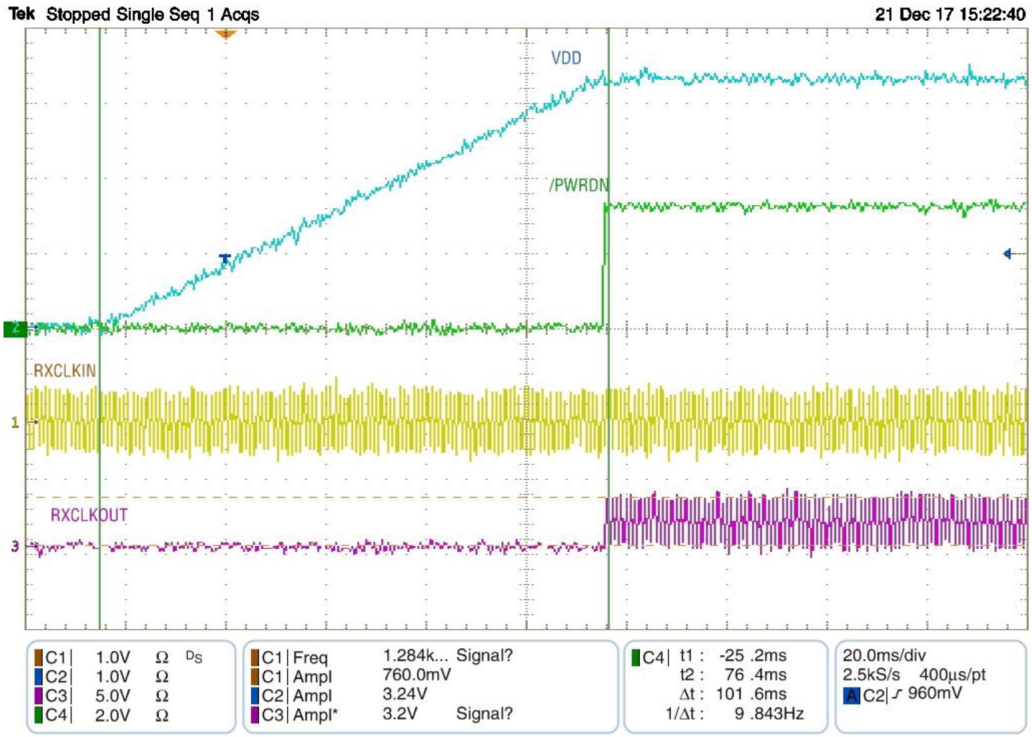

Figure 13: UT54LVDS218 Test #4 Typical PVT Corner Measured Waveform

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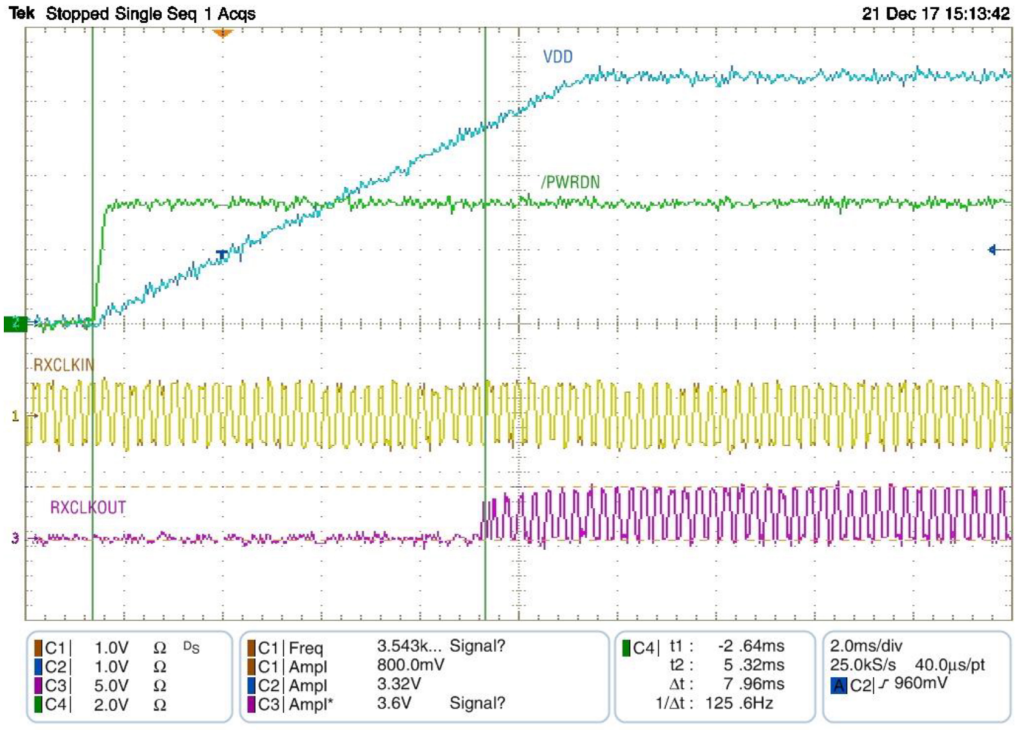

Figure 14: UT54LVDS218 Test #5 Typical PVT Corner Measured Waveform

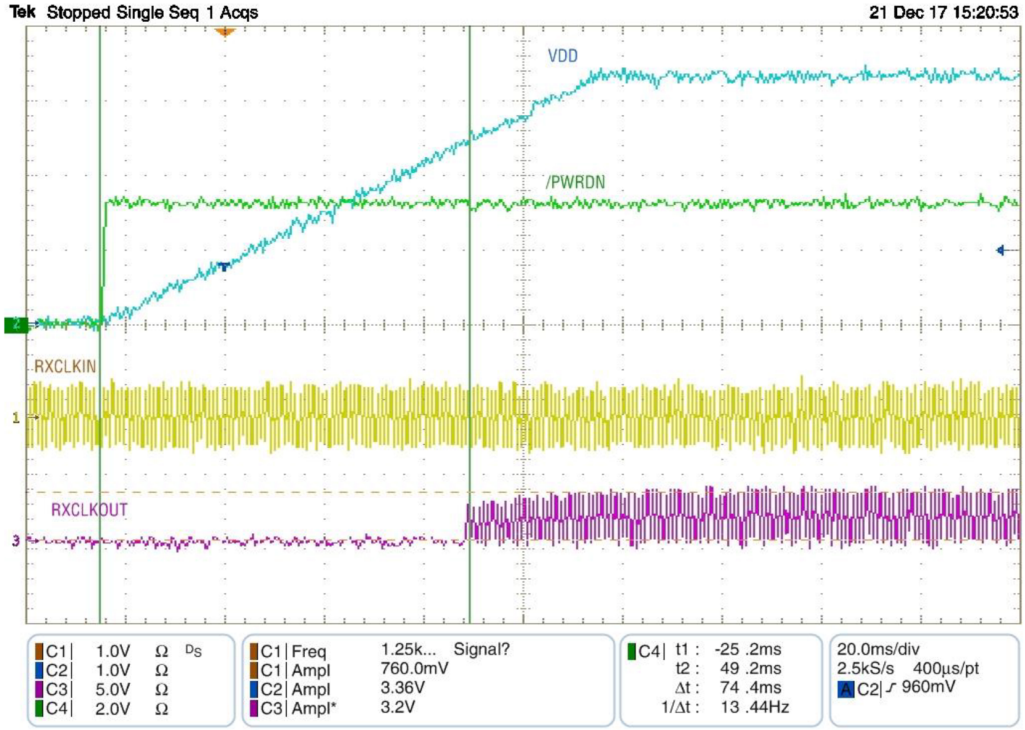

Figure 15: UT54LVDS218 Test #6 Typical PVT Corner Measured Waveform

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Revision History

Date	Rev. #	Author	Change Description
12/18/2017	1.0.0	SZ	Advanced Version
01/03/2018	1.0.1	SZ	Initial Release