APPLICATION NOTE

RELEASED 9/9/10

UT699-AN-02

UT699 External Memory Mapping

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC* Number:
UT699 32-bit Fault-Tolerant SPARC V8/LEON 3FT Processor	UT699	5962-08228	01, 02	WG07

* PIC = Product Identification Code

1.0 Introduction

This application note explains the external memory mapping of the UT699 with particular emphasis on the relationship between the memory space shared between SRAM and SDRAM. The purpose of this application note is to provide the system designer with the information necessary to develop an efficient memory architecture.

2.0 Memory Map Overview

Table 2 shows the UT699's external addressable memory space. Memory space is divided into three regions: PROM, memory mapped I/O, and SRAM / SDRAM. The PROM and memory mapped I/O chip select pins always decode the same address space. For the shared SRAM / SDRAM space, address decoding depends upon how the designer configures the memory. Valid configuration options are described in Section 2.1.

Table 2: UT699 Memory Mapping

Memory Area	Memory Range	Memory Select Pins
PROM	0x00000000 - 0x0FFFFFFF	$\overline{\text{ROMS[0]}}$
PROM	0x10000000 - 0x1FFFFFFF	$\overline{\text{ROMS[1]}}$
I/O	0x20000000 - 0x2FFFFFFF	$\overline{\text{IOS}}$
Reserved	0x30000000 - 0x3FFFFFFF	N/A
SRAM / SDRAM	0x40000000 - 0x7FFFFFFF	$\overline{\text{RAMS[4:0]}}$, $\overline{\text{SDCS[1:0]}}$

2.1 SRAM and SDRAM Configuration Options

SRAM and SDRAM share a 1GB memory space starting at address 0x40000000. The designer may choose to implement a system that uses SRAM only, SDRAM only, or a combination of the two. The DE and SI bits in Memory Configuration Register 2 (MCFG2) determine which type of memory will be interfaced to the UT699. Setting DE enables SDRAM and setting SI inhibits SRAM. Several different examples of memory interface options are shown below. The SZ field in MCFG2 determines the size of each SRAM bank except for the area decoded by $\overline{\text{RAMS[4]}}$, which always maps to the upper 512MB when SDRAM is not used. Accesses to $\overline{\text{RAMS[4]}}$ can be stretched using the $\overline{\text{BRDY}}$ signal. SDRAM bank and column sizes are determined by DZ and DS, respectively. For more information please refer to the document *UT699 User Manual* available at cobhamaes.com. The following tables illustrate several different memory configuration options based upon the states of SI and DE, and the SRAM bank size SZ.

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Table 3: SRAM-only Memory Map

Start Address	SRAM Bank Size		
	256MB	128MB	64MB
0x7C000000	$\overline{\text{RAMS[4]}}$	$\overline{\text{RAMS[4]}}$	$\overline{\text{RAMS[4]}}$
0x78000000			
0x74000000			
0x70000000			
0x6C000000			
0x68000000			
0x64000000			
0x60000000			
0x5C000000	$\overline{\text{RAMS[1]}}$	$\overline{\text{RAMS[3]}}$	UNUSED
0x58000000			
0x54000000		$\overline{\text{RAMS[2]}}$	
0x50000000			
0x4C000000	$\overline{\text{RAMS[0]}}$	$\overline{\text{RAMS[1]}}$	$\overline{\text{RAMS[3]}}$
0x48000000			$\overline{\text{RAMS[2]}}$
0x44000000		$\overline{\text{RAMS[0]}}$	$\overline{\text{RAMS[1]}}$
0x40000000			$\overline{\text{RAMS[0]}}$

Table 3 shows the case where only SRAM is used. **Note:** each SRAM chip select decodes an address range that is dependent upon the SRAM bank size. In the case of 256MB bank size, bank 4 has priority in the upper 512MB space and control signals for banks 2 and 3 are ignored. Table 4 indicates the register field settings for the three options shown above.

Table 4: Register Settings for SRAM-only Configuration

SRAM Bank Size	SI	DE	SZ
256MB	0	0	1111b
128MB	0	0	1110b
64MB	0	0	1101b

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Table 5: SRAM and SDRAM Memory Map

Start Address	SRAM Bank Size		
	256MB	128MB	64MB
0x7C000000	$\overline{SDCS[1]}$	$\overline{SDCS[1]}$	$\overline{SDCS[1]}$
0x78000000			
0x74000000			
0x70000000			
0x6C000000			
0x68000000			
0x64000000			
0x60000000			
0x5C000000	$\overline{RAMS[1]}$	$\overline{RAMS[3]}$	UNUSED
0x58000000			
0x54000000		$\overline{RAMS[2]}$	
0x50000000			
0x4C000000	$\overline{RAMS[0]}$	$\overline{RAMS[1]}$	$\overline{RAMS[3]}$
0x48000000			$\overline{RAMS[2]}$
0x44000000		$\overline{RAMS[0]}$	$\overline{RAMS[1]}$
0x40000000			$\overline{RAMS[0]}$

Table 5 shows the case where both SRAM and SDRAM are used. Address decoding is similar to the case of SRAM only, except that the upper 512MB of address space is used exclusively for SDRAM. In this configuration, $\overline{RAMS[4]}$ is never used.Table 6 indicates the register field settings for the three options shown above.

Table 6: Register Settings for SRAM and SDRAM Configuration

SRAM Bank Size	SI	DE	SZ	DZ
256MB	0	1	1111b	111b
128MB	0	1	1110b	111b
64MB	0	1	1101b	111b

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Table 7: SDRAM Memory Map

Start Address	SRAM Bank Size
	N/A
0x7C000000	$\overline{SDCS[1]}$
0x78000000	
0x74000000	
0x70000000	
0x6C000000	
0x68000000	
0x64000000	
0x60000000	
0x5C000000	$\overline{SDCS[0]}$
0x58000000	
0x54000000	
0x50000000	
0x4C000000	
0x48000000	
0x44000000	
0x40000000	

Table 7 shows the case where only SDRAM is used. $\overline{SDCS[0]}$ decodes the lower 512MB of address space and $\overline{SDCS[1]}$ decodes the upper 512MB. Table 8 indicates the register field settings for the case shown above.

Table 8:

SRAM Bank Size	SI	DE	SZ	DZ
N/A	1	1	don't care	111b

3.0 Design Examples

3.1 System with two SRAM Devices

The UT699 treats all memory as contiguous when code segments are not assigned to specific addresses. Therefore, extra address decoding might be necessary depending upon the size of the memory devices. An example is where the system interfaces with two SRAM devices, each having a logical size of 1MB (1024kB). The UT699 can be configured to select the SRAM devices using two bank select lines $\overline{RAMS[1:0]}$. Each bank size is set to 1024kB by setting the SZ field in MCFG2 to7 (0111b). Accesses to addresses 0x40000000 to 0x400FFFFF maps to the SRAM tied to $\overline{RAMS[0]}$; accesses to addresses 0x40100000 to 0x401FFFFF maps to the SRAM tied to $\overline{RAMS[1]}$.

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3.2 System with SRAM and SDRAM

An example of a split addressing scheme is where the .text segment is to be loaded from PROM and run in SRAM at address 0x40000000. The .data and .bss segments are to be located in SDRAM at address 0x60000000. Creating a PROM image involves two steps. A compiler such as the sparc-elf-gcc compiler could be used to first compile the code without linking. Then, the location of the code and data segments can be specified by passing the -Ttext=<address> and -Tdata=<address> options to the MKPROM2 utility e.g. -Ttext=0x40000000 and -Tdata=0x60000000. For more information, see the document *BCC - Bare-C Cross-Compiler User's Manual* available at cobhamaes.com.

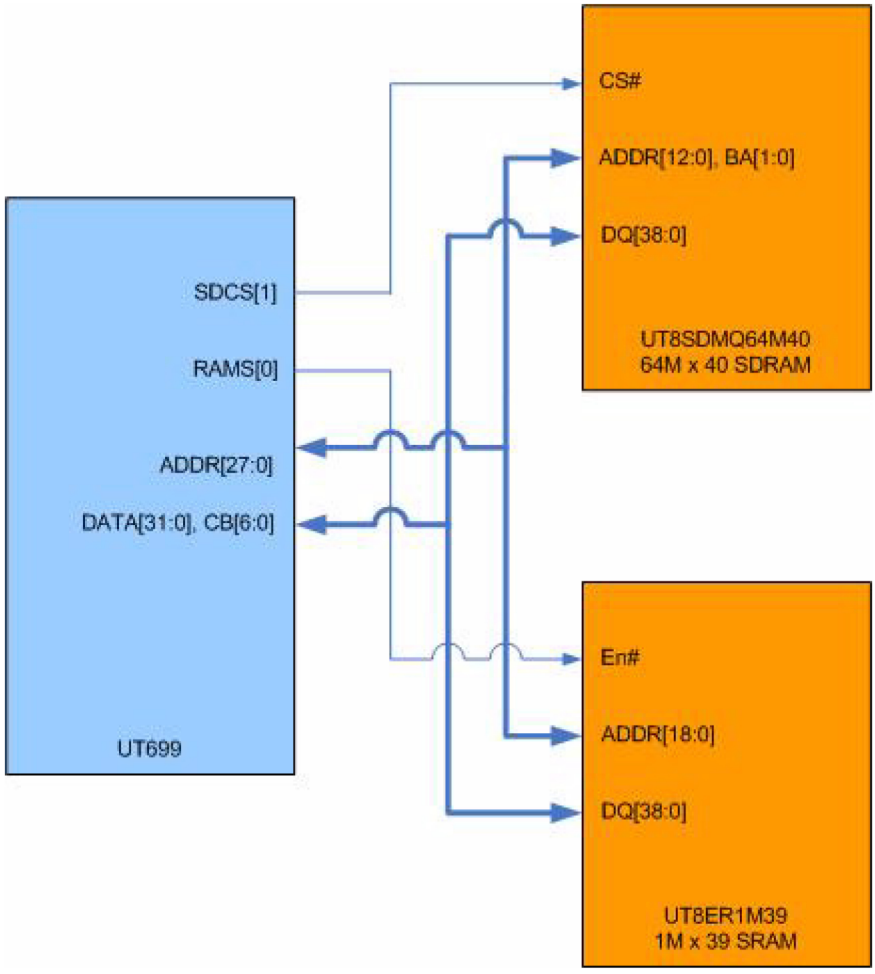

Figure 1. Block Diagram of a System Utilizing SRAM and SDRAM

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Figure 1 shows the interconnection of a system utilizing both SRAM and SDRAM. For simplicity, only the chip select lines $\overline{\text{SDCS[1]}}$ and $\overline{\text{RAMS[0]}}$ are shown. The SRAM chosen for this design has a data capacity of 4MB. The SDRAM is a multi-chip module that contains five devices, each organized as 16M x 8 x 4 where the bank size is 16MB and the column size is 2048. Total SDRAM is 2.5Gb with a configuration of 16M x 40 x 4, where the fifth device is used to store the EDAC check bits. Total addressable data, not including the EDAC check bits, is 256MB. Therefore, the bank select field DZ is set to 110b. Table 9 indicates the required fields for MCFG2 to achieve proper operation. **Note:** DS is don't care, as the default for this field is 2048 when DZ is 110b.

Table 9: Register Configuration for SRAM and SDRAM

Field	Value	Size
SZ	1001b	4MB
DE	1	--
SI	0	--
DZ	110b	256MB
DS	don't care	2048