DATASHEET

RELEASED 05/17/2022

32-Bit Arm® Cortex®-M0+ Microcontroller

UT32M0R500

Features

- Single 3.3 V Supply Voltage (3.0 V to 3.6 V)
- System
  - Arm® Cortex® M0+
  - Arm® Cortex® M0+ built-in NVIC
- Digital and Communication Peripherals
  - 2x CAN 2.0B Controllers
  - 2x UART
  - SPI
  - 2x I2C
  - JTAG
  - 4x General purpose timers
  - 3x PWM
  - Watchdog Timer
  - Real Time Clock
  - 48x GPIO (21 dedicated)
  - 8x Hardware Interrupts (shared with GPIO)
- Analog Peripherals
  - 12-bit ADC 100 ksps with PGA
    - 16 Single Ended or 8 Differential Channels
  - 1 mA Precision Current Source
  - 2x 12-bit DACs
  - 2x Analog Voltage Comparators
  - Temperature Sensor
- Power Control
  - Multiple power modes for low power optimization
  - System clock scalable for low power
- Memories
  - 96KB Dual Port SRAM with EDAC + Scrubbing
  - 64Mb Flash Memory
    - 384KB in 96KB increments for user firmware
- Clock Generation
  - 50 MHz internal clock factory-trimmed RC
  - Support for external clock source and crystal oscillator
- Offered in the CAES Constellation process flow, which includes tri-temp testing and radiation assurance, in the same packaging
- Standard Microelectronics Drawing (SMD):
  - 5962-17212 (QML Q and Q+)
- Package Options:
  - 143-Pin
    - Ceramic Land Grid Array
    - Ceramic Column Grid Array
    - Ceramic Ball Grid Array (Prototype Only)
    - Plastic Ball Grid Array (Preliminary, see Datasheet Definitions)
  - 14.5 x 14.5 mm, 1 mm pitch

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Operational Environment

- Temperature Range: -55°C to +105°C
- Total Dose: 50 krad(Si)
- SEL Immune: ≤ 80 MeV -cm^2/mg
- SER_{HI}: 8.30 × 10^{-8} errors/device-day

Applications

- CAN Bus Controller
- SpaceVPX Chassis Management
- Telemetry/System Health Monitoring
- Distributed Command and Control
- Data Acquisition
- RF Signal Chain Management

Introduction

The UT32M0R500 microcontroller utilizes the Arm® Cortex®-M0+ 32-bit processor with a RISC based architecture operating at a 50 MHz frequency. The microcontroller includes a memory protection unit (MPU), embedded memories, with several peripherals including support for CAN 2.0B. For increased design flexibility, the microcontroller includes several analog features such as an analog signal channel with a multiplexed input combined with a programmable gain amplifier and analog-to-digital converter, two digital-to-analog converters, two analog comparators, and precision current source.

The UT32M0R500 incorporates a variety of power-saving modes to facilitate the design of low-power applications.

The UT32M0R500 is supported by the Keil® Development Tool Environment. For information on the Arm® Cortex®-M0+ core please refer to the Arm® Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

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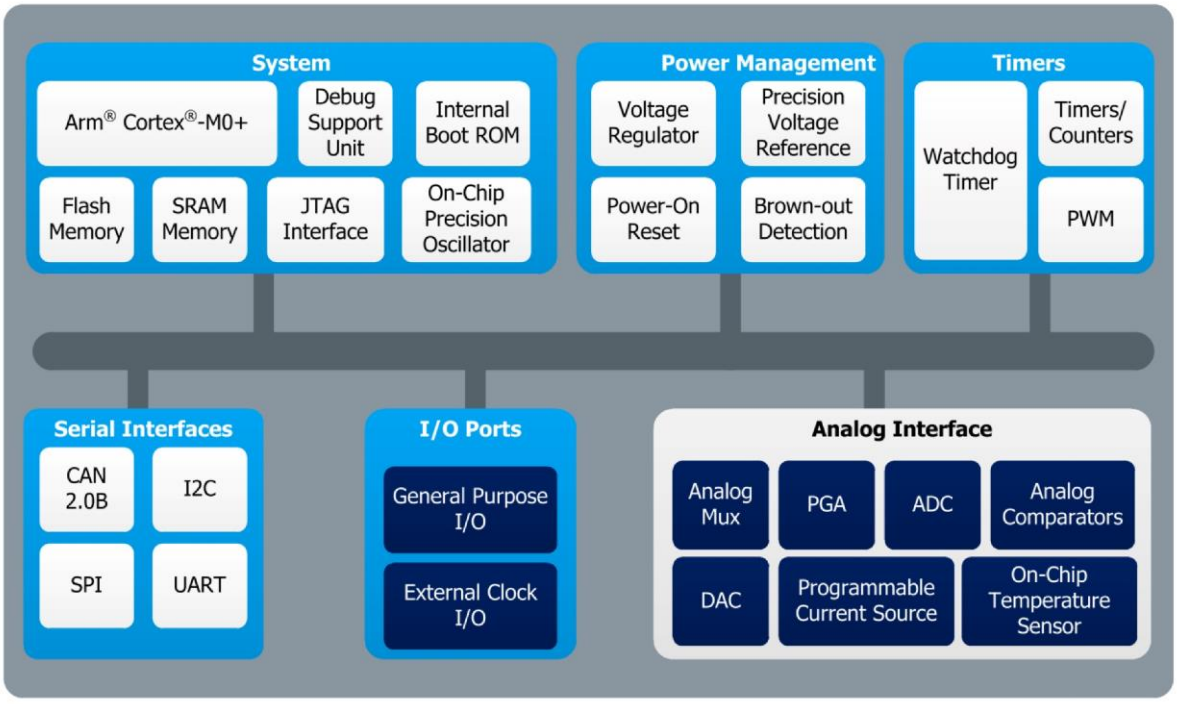

Figure 1: UT32M0R500 Block Diagram

32-Bit Arm® Cortex®-M0+ Microcontroller

UT32M0R500

1 Functional Overview/System Summary

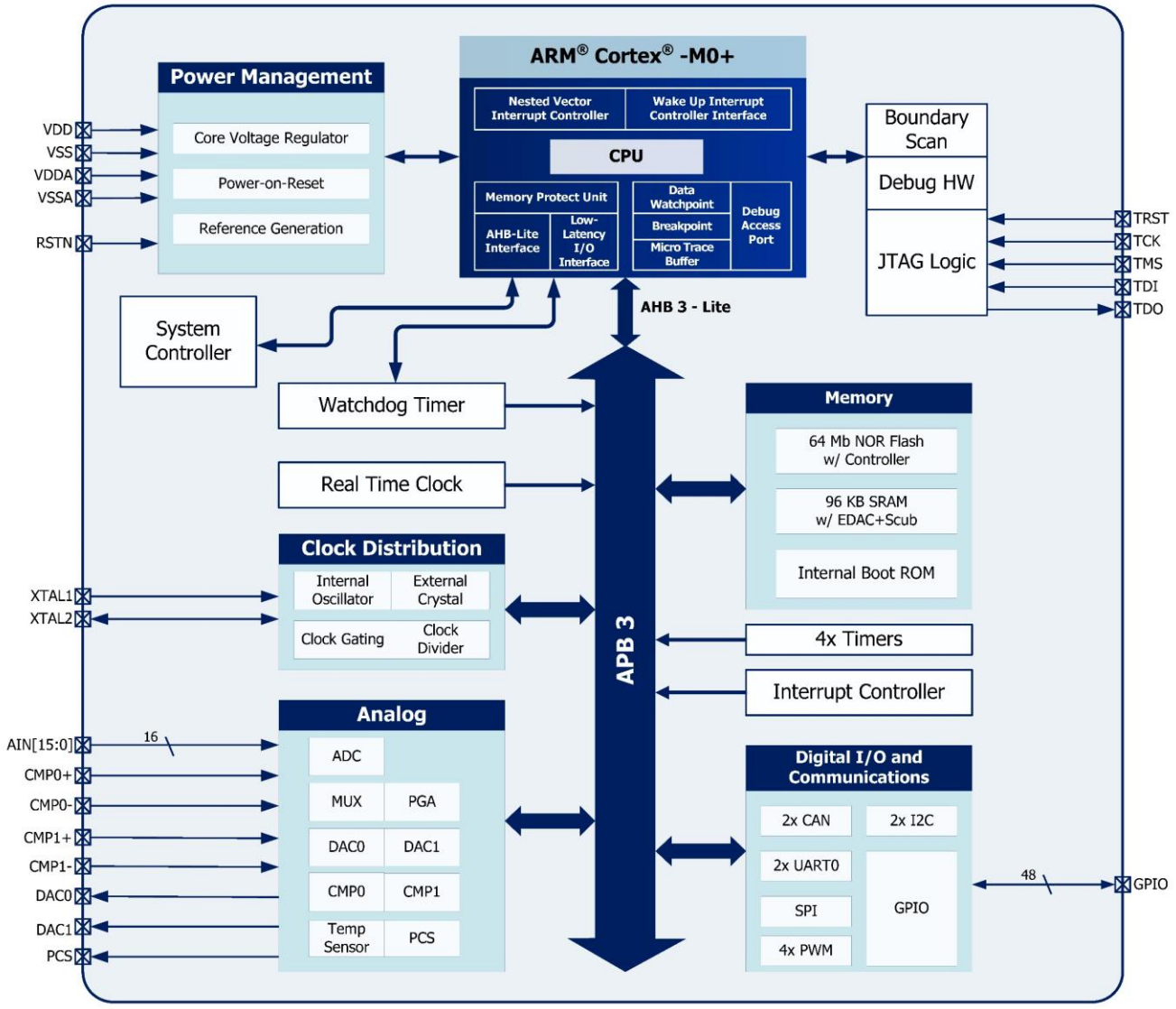

Figure 2: UT32M0R500 Functional Block Diagram

1.1 Arm® Cortex®-M0+ Processor with MPU

The Cortex-M0+ processor is a low-power 32-bit ARM Cortex processor designed for a wide range of embedded applications. The Cortex-M0+ is based on a highly optimized 32-bit processor core with a pipeline V on Neumann architecture. The processor has exceptional energy efficiency with a small but powerful instruction set coupled with a hardware single-cycle multiplier and Memory Protection Unit (MPU).

With the use of the Arm core, the UT32M0R500 is compatible with the Arm tools and software.

Table 1: UT32M0R500 Cortex-M0+ Configuration

Features	ARM M0+ Configurable Option	UT32M0R500 Configuration
Interrupts	0 – 32	32
Data Endianness	Little-endian or big-endian	Little-endian
SysTick Timer	Present or absent	Present
Number of Watchpoint Comparators	0, 1, 2	2
Number of Breakpoint Comparators	0 - 4	4
Multiplier	Fast or small	Fast (Single Cycle)
Wakeup Interrupt Controller	Supported or not support	Supported
Vector Table offset Register	Present or absent	Present
Unprivileged/Privileged Support	Present or absent	Present
Memory Protection Unit	Present or absent	Present
Reset All Registers	Present or absent	Present
Debug Configuration	Present or absent	Present
Micro Trace Buffer	Present or absent	Present

1.2 Core –M0+ Peripherals

1.2.1 SysTick

The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).

1.2.2 Nested Vector Interrupt Controller (NVIC)

The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC includes a Non-Maskable Interrupt (NMI), zero jitter interrupt capability, and four interrupt priority levels with 32 programmable interrupts.

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on bank 0, bank 2, or bank 3 regardless of the selected function can be programmed to generate an interrupt on a rising edge, a falling edge, high or low state.

1.2.3 Micro Trace Buffer

The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

1.3 Low Power Options

The UT32M0R500 includes built-in flexibility for low power operation. This is supported through power down control for several of the IP blocks in the device.

1.4 System Controller

The UT32M0R500 includes a system controller that provides functionality to support the miscellaneous functions without dedicated controllers. This includes items such as:

- Reset status – Last reset source, reset counter
- Power Management Unit (PMU) Enable
- Reset control logic
- Boot Configuration Access
- Clock Divide Control
- Oscillator Shutdown
- Analog Shutdowns for
  - Precision current source
  - Temperature Sensor shutdown
  - Low Noise Voltage Reference to ADC/DAC/Comparators shutdown
  - Current reference to ADC/DAC/Comparators shutdown
- General Purpose Registers with "Stay Alive" option

The UT32M0R500 has a clock distribution unit (CDU) that supports both an internal and external clock source. The internal clock source is based on a highly robust 50 MHz oscillator. The CPU and each peripheral have a clock divider circuit that is controlled by the system controller. The CDU supports a crystal oscillator or square wave input on the XTAL1 and XTA2 pins for the external clock source.

The clock selection is based on the state of the CLKSEL pin (0 = internal, 1 = external) which is read at the end of the boot sequence.

1.5 Power Management

1.5.1 On-Chip Regulators

The UT32M0R500 includes on-chip regulators for supplying power to the digital core, oscillator, and analog components. CAES recommends separate digital power analog power planes (power and ground) to minimize noise interference. For more information, see the UT32M0R500 Board Design Recommendations appnote on the CAES website:

https://caes.com/product/ut32m0r500#downloads

1.5.2 Power-on-Reset

The UT32M0R500 contains power-on-reset (POR) circuitry. The POR monitors the VDD and VDDA power supplies. The POR also monitors the internally regulated core voltage (VDDC). The POR supports an external reset mode using the RSTN pin.

1.6 Boot Modes

The UT32M0R500 supports four (3) modes of booting the device where the mode selection is based on the configuration of the BOOTCFG0 and BOOTCFG1 pins as specified in Table 2.

Table 2: Boot Mode Selection Description

Boot mode selection pins		Boot Mode	Description
BOOTCFG1	BOOTCFG0		
0	0	0	Load image from internal Flash memory into SRAM and execute
0	1	1	Reserved
1	0	2	Load/Update image over UART0 into flash (reset required)
1	1	3	Load/Update image over CAN0 into flash (reset required)

Note:

1) Boot modes will only be switched or interpreted on a RESET event or external reset.

The following sections give further details of the three boot modes supported by the UT32M0R500.

1.6.1 Boot Mode 0 (BOOTCFG = 2'b00)

This mode describes the loading of the firmware image from NOR Flash into internal SRAM memory operation. This mode is considered the normal (default) boot operation mode. In this mode, the bootloader performs a system initialization where the device is placed in the default state and initializes communication with the NOR Flash. The bootloader copies the firmware image from NOR Flash memory to internal SRAM. After copying the user code, a CRC verification of the code is performed to determine if the transfer was successful. Upon a successful code transfer, the bootloader checks the CLKSEL pin to determine if an external clock is to be used. If the CLKSEL pin is in a High state, then the system clock is switched over to using the external clock on the XTAL[1:0] pins. All bootloader operations are performed using the internal oscillator operating at 50 MHz until the CLKSEL pin is checked. After the clock selection is performed, the program counter is set to point to the beginning of the transferred code and code execution starts.

1.6.2 Boot Mode 1 (BOOTCFG = 2'b01)

Reserved.

1.6.3 Boot Mode 2 (BOOTCFG = 2'b10)

This mode describes the loading of the firmware image over UART (UART0) mode of operation. In this mode, the bootloader first performs a system initialization where the device is placed in the default state. The bootloader then configures the UART0 for operating at 19200 baudrate/x-bits/x-parity/stop bit. After configuring the UART0, the bootloader loads the firmware image transmitted over UART0 to the addressed memory of the internal Flash memory location based on the image number selected. All bootloader operations are performed using the internal oscillator operating at 50 MHz. To execute the firmware, the BOOTCFG pins must be set to 2'b00 and a reset applied.

1.6.4 Boot Mode 3 (BOOTCFG = 2'b11)

This mode describes the loading of the firmware image over the CAN bus (CAN0) mode of operation. In this mode, the bootloader first performs a system initialization where the device is placed in the default state. The bootloader

then configures the CAN0 for operating at 125 kHz. After configuring the CAN0, the bootloader copies the firmware image transmitted over CAN0 to the addressed location as prescribed by the image number. After a successful load of the firmware, the BOOTCFG pins must be set to 2'b00 and a reset applied for the firmware to start executing. All bootloader operations are performed using the internal oscillator operating at 50 MHz.

1.7 GPIO – General Purpose Inputs/Outputs

The pins of the UT32M0R500 support operating as general purpose I/O or as alternative functions. Configuration registers control the functionality of the pin and its connectivity to the on-chip peripherals for the alternate functions. When configuring for use as the alternative function, the peripheral should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Dedicated GPIO are initialized as input, whereas GPIO with alternate functions are initialized to use the alternate function. The GPIO are configured in three banks of 16 pins each: Bank 0[15:0] = GPIO[15:0], Bank 1[15:0] = GPIO[31:16], Bank 2[15:0] = GPIO[47:32] in MSB:LSB order for each bank. Each bank has a shared interrupt (for the 16 pins within the bank). In addition, each of the inputs to the GPIO (when configured as input) can be used as an IRQ. All pins can be configured to have a pull-up, pull-down, or tri-state (for open-drain operation). The GPIO are half-word (16 bit), byte (8 bit) or half-byte (4 bit) addressable where read or writes occur in a single cycle. The GPIO support upper/lower byte mask registers for access control.

Table 3: GPIO Reference

GPIO number	Bankx[15:0]	Bank AHB Address
GPIO 2 = GPIO[47:32]	Bank 2	0x40022000 – 0x40022FFF
GPIO 1 = GPIO[31:16]	Bank 1	0x40021000 – 0x40021FFF
GPIO 0 = GPIO[15:0]	Bank 0	0x40020000 – 0x40020FFF

The GPIO pins have the following features:

- State programmable
- After power-up the dedicated I/O pins are configured as inputs. All other pins are configured to use the alternate function.
- Most digital pins can be a peripheral function or be driven by GPIO logic
- GPIO logic organized into banks of 16 pins
- GPIO can be software controlled to be high, low, tri-state, pull-up or pull-down
- GPIO can be programmed to generate a shared interrupt for any pin for each bank
- Stay alive functionality supported

1.8 Memory

1.8.1 On-chip Flash Memory

The UT32M0R500 contains 64Mb of on-chip flash program memory. The flash memory has 384KB dedicated for user application firmware allocated in increments of 96KB. The flash memory can be programmed through the UART0 or CAN0 interfaces.

Further details about the flash memory can be referenced in the UT32M0R500 User/Functional Manual.

1.8.2 On-chip SRAM

The UT32M0R500 includes a total of 96KB on-chip dual-port static RAM (SRAM) data memory to be used for firmware and data. The dual port architecture, which consists of a single memory array, supports access from two independent ports – each having a set of address, data, and control signals. The device allows simultaneous access to a single SRAM memory location from both ports. The SRAM allocates 96KB of memory for user application firmware accessible by the CPU. The SRAM includes error detection and correction (EDAC) with bit scrubbing. The EDAC implements a Single Error Correction Double Error Detection (SECDED) protection algorithm. The SRAM module includes provisions for providing single bit error (SBE) and multiple bit error (MBE) counts for user processing with programmable interrupt support for the MBE.

Note: Only 90KB of SRAM is available during boot with the full 96KB available during program execution.

1.8.3 MPU

The UT32M0R500 has a Memory Protection Unit (MPU) which can be used to improve the robustness of an embedded system by protecting critical data within the user application. The MPU divides the memory map into a number of regions with privilege permissions and access rules preventing disallowed accesses.

1.9 Analog Components

1.9.1 12-bit Analog-to-Digital Converter

The UT32M0R500 contains one ADC. It is a single 12-bit Delta Sigma ADC with 16 input channels and programmable gain amplifier. It has the following features:

- 12-bit Output Data
- Selectable Oversample Rate of Delta Sigma Modulator
- Up to 100 ksps conversion rate
- APB-protocol control and status access from M0+ system bus
- Input multiplexing among sixteen pins
- Supports auto-sequence of 17 signal inputs, or a single input enable
- Single-ended or differential inputs controlled by enable registers
- Programmable gain amp enable and gain setting, SINC4 filter enable per channel
- Two selectable decimation filters (COI3 or SINC4)
- Individual result register for each input channel
- Programmable gain amplifier
- Power-down mode

1.9.2 12-bit Digital-to-Analog Converters

The UT32M0R500 contains two voltage output DACs. Each of the DACs operates independently and allow for generating a variable analog output. The maximum output of each DAC is VREFP. Each DAC has the following features:

- Buffered output
- Synchronous or Independent update
- Power-down mode
- Soft-Reset supported by enable bit

1.9.3 Comparators

The UT32M0R500 contains two high speed comparators with hysteresis.

1.10 Pulse Width Modulators

The UT32M0R500 contains three standard 16-bit PWMs. The modules are multi-purpose timer/counter systems allowing for complex timing or waveform generation. The PWM has an internal prescalar.

- Each PWM has three individual outputs, or two paired (Push/Pull) Outputs
- Programmable Dead-Band Scaler
  - Can divide the system clock up to a total dead band range of 20ns to 81,920ns
- Programmable Clock Scaler per PWM Individual Output
  - Support a 335 ms pulse
- Single Combined Interrupt for all three PWMs
- Interrupt counter to reduce M0+ ISR activity

1.11 General Purpose Timers

The UT32M0R500 includes four 32-bit programmable timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, or perform other actions at specified timer values. Each of the timers support three modes of operation: free-running, periodic (with interrupt), one-shot (interrupt and halt)

1.11.1 Real-Time Clock

- Programmable 32-bit free-running up-counter
- Clocked only by system clock (Not truly "real time")
- Current Value register can be read through APB interface
- Counter wrap at value = match register, or at maximum count
- Counter wrap to a "load register" value

1.11.2 WDT – Watchdog Timer

The UT32M0R500 includes a Watchdog Timer (WDT) which is a system for monitoring correct program operation. The WDT supports two modes of operation: Timeout and Window. In Timeout mode, the WDT is configured to a predefined time-out period and is constantly running when enabled. If the WDT is not cleared within the time-out period, it will issue a system reset. In Window mode, the WDT has a defined window within the total time-out period during which the WDT must be cleared. If the WDT is cleared outside this window, either too early or too late, a system reset will be issued.

- A system (soft)reset is issued if the WDT is not cleared before its time-out period
- Two modes of operation
  - Timeout
  - Window
- 32 bit Selectable time-out periods (both Timeout and Window Modes)
- Circuit meant to detect stuck or runaway code and restore system to functionality
- Countdown timer that generates first an interrupt then a system reset if not cleared
- Window mode will reset system if the timer is cleared before a programmable count

1.12 Communication Interfaces

1.12.1 CAN – Controller Area Network (CAN0, CAN1)

In the UT32M0R500, there are two independent CAN controller peripherals. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of robustness and reliability. Each of the CAN controllers is based on the Philips SJA1000 and supports both BasicCAN (CAN 2.0A) and PeliCAN (CAN 2.0B) mode with a few exceptions. Each mode of operation utilizes a 64-byte RX buffer and 8-byte TX buffers. The mode of operation is user selectable through the Clock Divider register. Each CAN controller operate independently with the following features:

- CAN 2.0B supported with max speed of 1 Mbps.
- Based on the Philips SJA1000 and has a compatible register map with a few exceptions.
- Supports both BasicCAN (PCA82C200 like) and PeliCAN mode.
- In PeliCAN mode the extended features of CAN 2.0B is supported.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- 64-byte RX Buffer, 8-Byte TX Buffer.
- 32 user configurable registers.
- Includes acceptance filters with support mask filters.

Further details about the CAN interface can be referenced in the UT32M0R500 User/Functional Manual.

1.12.2 I2C (I2C0, I2C1)

The UT32M0R500 contains two I2C controllers. The I2C-bus is a simple 2-wire serial multi-master bus with collision detection and arbitration. The bus consists of a serial data line (SDA) and a serial clock line (SCL). Each I2C interface is Standard Mode (Sm, up to 100 kbit/s) compliant and Fast Mode (Fm, up to 400 kbit/s), Fast Mode Plus (Fm+, up to 1 Mbit/s) compatible. Each of the interfaces support 7-bit and 10-bit addressing modes, with a user-selectable bit filtering length.

- Standard (up to 100 kbps), Fast (up to 400 kbps), and Fast+ (1 Mbps) transfer speeds.
- Two wire serial communication: Serial Clock Line(SCL) for clock and Serial Data Line(SDA) for data
- Supports master or slave mode of operations
- Collision detection and clock synchronization procedure for multi master bus operation
- Supports 7-bit or 10-bit addressing
- User-selectable bit filtering length
- Dynamic updating of I2C address without losing the bus
- 14 maskable interrupts combined to one M0+ interrupt

1.12.3 SPI – Serial Peripheral Interface

The UT32M0R500 contains one SPI controller. The SPI controller is capable of operation on a SPI bus. It can interact with multiple slaves on the bus. Only a single master and a single slave can communicate on the bus. The SPI controller has the following features:

- SPI Master operation using Motorola SPI protocol
- Up to 10 MHz transfer rate
- Tx and Rx FIFOs with a 16 word depth
- User-selectable SPI data width of 4-16 bits
- Programmable RX sample point delay, to support long transmission lines
- User-selectable SPI Baud rate, at even-integer division of system clock
- Supports all 4 SPI SCPH and SCPOL modes
- Supports EEPROM read mode
- Supports up to 3 slave selects

1.12.4 UART – Universal Asynchronous Receiver-Transmitter (UART0, UART1)

The UT32M0R500 contain two UARTs. Standard baud rates such as 115200 Bd can be achieved without the need for external crystal.

- Independent transmit and receive for each of the modules
- 8-bit Data
- Supports parity bit and one stop bit
- Low pass filter on start bit

1.13 Memory Map

Table 4. AHB Memory Map Table

Address Range	UT32M0R500 Modules
0x0000 0000 - 0x0000 7FFF (32KB)	Boot ROM
0x0100 0000 - 0x0100 FFFF (64KB)	NOR Flash
0x2000 0000 - 0x2001 7FFF (96KB)	SRAM
0x4000 0000 - 0x4001 FFFF (128KB)	APB Peripherals
0x4002 0000 - 0x4002 0FFF (4KB)	AHB GPIO Bank 0
0x4002 1000 - 0x4002 1FFF (4KB)	AHB GPIO Bank 1
0x4002 2000 - 0x4002 2FFF (4KB)	AHB GPIO Bank 2
0x4002 3000 - 0x4002 3FFF	AHB CAN 0
0x4002 4000 - 0x4002 4FFF	AHB CAN 1
0x4002 FFFF - 0x4002 F000 (4KB)	System Controller
0xE000 0000 - 0xE00F FFFF	Private peripheral bus addresses in the Cortex-M0+
0xF000 0000 - 0xF000 0FFF (4KB)	System ROM
0xF020 0000 - 0xF020 0FFF (4KB)	MTB SFR
0xF021 0000 - 0xF021 FFFF (64KB)	4kB MTB SRAM
0xF022 0000 - 0xFFFF FFFF	Cortex M0+

Table 5. APB Peripheral Memory Map Table

Address Range	UT32M0R500 Modules
0x4000 0000 - 0x4000 0FFF	RTC
0x4000 1000 - 0x4000 1FFF	Dual Timer0
0x4000 2000 - 0x4000 2FFF	Dual Timer1
0x4000 3000 - 0x4000 3FFF	PWM
0x4000 4000 - 0x4000 4FFF	UART0
0x4000 5000 - 0x4000 5FFF	UART1
0x4000 6000 - 0x4000 6FFF	SPI
0x4000 7000 - 0x4000 7FFF	DACs
0x4000 8000 - 0x4000 8FFF	Watchdog
0x4000 9000 - 0x4000 9FFF	I2C0
0x4000 A000 - 0x4000 AFFF	I2C1
0x4000 B000 - 0x4000 BFFF	Trim Control
0x4000 C000 - 0x4000 CFFF	NFC (NOR Flash Controller)
0x4000 D000 - 0x4000 DFFF	SRAM EDAC/Scrub
0x4000 E000 - 0x4000 EFFF	Comparators
0x4000 F000 - 0x4000 FFFF	ADC

2 Pinlist

Abbreviation	Description
IPU	LVTTL Compatible
I/O	LVCMOS Compatible Tri-State Bi-Direct with Internal Pull-up/Pull-down
I	LVCMOS Compatible Input
O	LVCMOS Compatible Output
AI	Analog Input
AO	Analog Output
SN	Selectable Pull-up/Pull-down, neither selected on power-up
NC	No connect. Required for pin to remain floating.
X	Unknown
Z	Tri-State, Floating or High Impedance
NUIL	Not used input low. Need to be connected by user to V_{SS} through a ≥10 kΩ±10% resistor

Table 6: Pinlist

Pin No.	Name	Type	Default State	Value During POR	Reset Value After POR	PU/PD	Description
D5, E5, E7, F5, F7, G5, G7, H5, H7, J5, J7	V_{DD}(3)	Power	-	-	-	-	Digital Supply voltage
C5, D4, E4, E6, F4, F6, G4, G6, H4, H6, J4, J6	V_{SS}(3)	Ground	-	-	-	-	Digital Ground
C6, C8, D6, D8, E8, F8, G8, H8, J8, K8, L8	V_{DDA}(3)	Power	-	-	-	-	Analog Supply Voltage
C7, 9, D7, D9, E9, F9, G9, H9, J9, K9, L9	V_{SSA}(3)	Ground	-	-	-	-	Analog Ground
E12	AIN0	AI	Input	X	Z	-	Analog Input Channel 0
F12	AIN1	AI	Input	X	Z	-	Analog Input Channel 1
G12	AIN2	AI	Input	X	Z	-	Analog Input Channel 2
H12	AIN3	AI	Input	X	Z	-	Analog Input Channel 3
F11	AIN4	AI	Input	X	Z	-	Analog Input Channel 4
G11	AIN5	AI	Input	X	Z	-	Analog Input Channel 5
H11	AIN6	AI	Input	X	Z	-	Analog Input Channel 6
J11	AIN7	AI	Input	X	Z	-	Analog Input Channel 7
J12	AIN8	AI	Input	X	Z	-	Analog Input Channel 8
K12	AIN9	AI	Input	X	Z	-	Analog Input Channel 9
L12	AIN10	AI	Input	X	Z	-	Analog Input Channel 10
M12	AIN11	AI	Input	X	Z	-	Analog Input Channel 11
K11	AIN12	AI	Input	X	Z	-	Analog Input Channel 12
L11	AIN13	AI	Input	X	Z	-	Analog Input Channel 13
M11	AIN14	AI	Input	X	Z	-	Analog Input Channel 14
M10	AIN15	AI	Input	X	Z	-	Analog Input Channel 15
J10	*Reserved*	-	-	-	-	-	*NC*
E11	*Reserved*	-	-	-	-	-	*NC*
D10	LDO 15_BYP	I	Input	-	-	-	Connect to VSSA
C10	LDO 28_BYP	I	Input	-	-	-	Connect to VSSA
F10	*Reserved*	-	-	-	-	-	*NC*
E10	*Reserved*	-	-	-	-	-	*NC*
G10	*Reserved*	-	-	-	-	-	*NC*
M9	PCS	O	Output	-	-	-	Precision Current Source Output
D12	DAC0	AO	Output	X	0	-	DAC Output Channel 0
C12	DAC1	AO	Output	X	0	-	DAC Output Channel 1

Pin No.	Name	Type	Default State	Value During POR	Reset Value After POR	PU/ PD	Description
B12	CMP0+	AI	Input	X	Z	-	Voltage Comparator 0 Positive Input
A12	CMP0-	AI	Input	X	Z	-	Voltage Comparator 0 Negative Input
D11	CMP1+	AI	Input	X	Z	-	Voltage Comparator 1 Positive Input
C11	CMP1-	AI	Input	X	Z	-	Voltage Comparator 1 Negative Input
M4	C AN0_RXD	I	Input	X	0	SN	CAN 0 Receive Data
M5	C AN0_TXD	O	Output	X	1	SN	CAN 0 Transmit Data
M6	UART0_TXD	O	Output	X	1	SN	UART 0 Channel Transmit Data
M7	UART0_RXD	I	Input	X	Z	SN	UART 0 Channel Receive Data
A2	CAN1_RXD GPIO32	I I/O	CAN1_RXD (Input)	X	Z	SN SN	CAN 1 Receive Data General purpose digital input/output
B1	CAN1_TXD GPIO33	O I/O	CAN1_TXD (Output)	X	1	SN SN	CAN 1 Transmit Data General purpose digital input/output
C1	UART1_TXD GPIO34	O I/O	UART1_TXD (Output)	X	1	SN SN	UART 1 Channel Transmit Data General purpose digital input/output
D1	UART1_RXD GPIO35	I I/O	UART1_RXD (Input)	X	Z	SN SN	UART 1 Channel Receive Data General purpose digital input/output
E1	SCL0 GPIO36	I/O I/O	SCL0 (Input)	X	Z	SN SN	I2C 0 Serial Clock General purpose digital input/output
F1	SDA0 GPIO37	I/O I/O	SDA0 (Input)	X	Z	SN SN	I2C 0 Serial Data General purpose digital input/output
J1	SCL1 GPIO38	I/O I/O	SCL1 (Input)	X	Z	SN SN	I2C 1 Serial Clock General purpose digital input/output
K1	SDA1 GPIO39	I/O I/O	SDA1 (Input)	X	Z	SN SN	I2C 1 Serial Data General purpose digital input/output
L1	SCLK GPIO40	I/O I/O	SCLK (Output)	X	0	SN SN	SPI Master Clock General purpose digital input/output
M1	MOSI GPIO41	I/O I/O	MOSI (Input)	X	Z	SN SN	SPI Master Output, Slave Input General purpose digital input/output

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Pin No.	Name	Type	Default State	Value During POR	Reset Value After POR	PU/ PD	Description
M2	MISO GPIO42	I/O I/O	MISO (Input)	X	Z	SN SN	SPI Master Input, Slave Output General purpose digital input/output
M3	SSN0 GPIO43	O I/O	SSN0 (Output)	X	1	SN SN	SPI Slave 0 Select General purpose digital input/output
B2	PWM0 GPIO44	O I/O	PWM0 (Output)	X	0	SN SN	Pulse Width Modulated Signal 0 General purpose digital input/output
B3	PWM1 GPIO45	O I/O	PWM1 (Output)	X	0	SN SN	Pulse Width Modulated Signal 1 General purpose digital input/output
C2	PWM2 GPIO46	O I/O	PWM2 (Output)	X	0	SN SN	Pulse Width Modulated Signal 2 General purpose digital input/output
C3	PWM3 GPIO47	O I/O	PWM3 (Output)	X	0	SN SN	Pulse Width Modulated Signal 3 General purpose digital input/output
D2	GPIO0	I/O	Input	X	Z	SN	General purpose digital input/output
D3	GPIO1	I/O	Input	X	Z	SN	General purpose digital input/output
E2	GPIO2	I/O	Input	X	Z	SN	General purpose digital input/output
E3	GPIO3	I/O	Input	X	Z	SN	General purpose digital input/output
F2	GPIO4	I/O	Input	X	Z	SN	General purpose digital input/output
F3	GPIO5	I/O	Input	X	Z	SN	General purpose digital input/output
G2	GPIO6	I/O	Input	X	Z	SN	General purpose digital input/output
G3	GPIO7	I/O	Input	X	Z	SN	General purpose digital input/output
H2	GPIO8	I/O	Input	X	Z	SN	General purpose digital input/output
H3	GPIO9	I/O	Input	X	Z	SN	General purpose digital input/output
J2	GPIO10	I/O	Input	X	Z	SN	General purpose digital input/output

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Pin No.	Name	Type	Default State	Value During POR	Reset Value After POR	PU/ PD	Description
J3	GPIO11	I/O	Input	X	Z	SN	General purpose digital input/output
K2	GPIO12	I/O	Input	X	Z	SN	General purpose digital input/output
K3	GPIO13	I/O	Input	X	Z	SN	General purpose digital input/output
L2	GPIO14	I/O	Input	X	Z	SN	General purpose digital input/output
L3	GPIO15	I/O	Input	X	Z	SN	General purpose digital input/output
B10	GPIO16 INTR17	I/O I	GPIO16 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 17
B9	GPIO17 INTR18	I/O I	GPIO17 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 18
B8	GPIO18 INTR19	I/O I	GPIO18 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 19
B7	GPIO19 INTR20	I/O I	GPIO19 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 20
B6	GPIO20 INTR21	I/O I	GPIO20 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 21
B5	GPIO21 INTR22	I/O I	GPIO21 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 22
B4	GPIO22 INTR23	I/O I	GPIO22 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 23
A3	GPIO23 INTR24	I/O I	GPIO23 (Input)	X	Z	SN SN	General purpose digital input/output External interrupt 24
A11	GPIO24 CMP0OUT	I/O O	GPIO24 (Input)	X	Z	SN SN	General purpose digital input/output Comparator 0 Output
A10	GPIO25 CMP1OUT	I/O O	GPIO25 (Input)	X	Z	SN SN	General purpose digital input/output Comparator 1 Output
A9	GPIO26 RTCK	I/O O	GPIO26 (Input)	X	Z	SN SN	General purpose digital input/output Real-time clock output

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Pin No.	Name	Type	Default State	Value During POR	Reset Value After POR	PU/PD	Description
A8	GPIO27 SSN1	I/O O	GPIO27 (Input)	X	Z	SN SN	General purpose digital input/output SPI Slave 1 Select
A7	GPIO28 SSN2	I/O O	GPIO28 (Input)	X	Z	SN SN	General purpose digital input/output SPI Slave 2 Select
A6	GPIO29 SSNM	I/O I	GPIO29 (Input)	X	Z	SN SN	General purpose digital input/output SPI Slave input for multi-master select
A5	GPIO30	I/O	Input	X	Z	SN	General purpose digital input/output
A4	GPIO31	I/O	Input	X	Z	SN	General purpose digital input/output
H1	XTAL1	I	Input	-	-	-	External Clock Signal Input (Crystal or Oscillator)
G1	XTAL2	O	Output	-	-	-	External Clock Signal Crystal Feedback
K6	*Reserved*	-	-	-	-	-	*NUIL*
B11	*Reserved*	-	-	-	-	-	*NUIL*
K4	TRST (1)(2)	I	Input	-	-	SN	JTAG Reset; Active LOW
L7	TMS (1)(2)	I	Input	-	-	-	JTAG Test Mode Select
L6	TCK (1)(2)	I	Input	-	-	SN	JTAG Clock Signal
K5	TDI (1)(2)	I	Input	-	-	SN	JTAG Data Input
L4	TDO (1)(2)	O	Output	X	0	-	JTAG Data Output
L10	CLKSEL	I	Input	-	-	SN	System Clock Select (Internal = Active LOW, External = Active HIGH)
K10	RSTN	I	Input	-	-	SN	Pin for system reset; Active LOW
M8	BOOTCFG [0]	I	Input	-	-	SN	Select Boot Mode Bit 0
K7	BOOTCFG [1]	I	Input	-	-	SN	Select Boot Mode Bit 1
L5	*Reserved*	-	-	-	-	-	*NUIL*
H10	*Reserved*	-	-	-	-	-	*NC*
C4	*Reserved*	-	-	-	-	-	*NC*

Notes:

1) When JTAG is being used for debugging, 10K pullup resistors should be placed upon the TRST, TMS, TCK, and TDI signals, with TDO floating. When JTAG is NOT being used (Ex. During Flight) TRST MUST have a 10K pulldown resistor, TMS, TCK, and TDI should stay pulled up, and TDO should stay floating.
2) The Keil ULINK2 JTAG pod has a variety of pin headers. Please ensure the correct signals are in use. (Ex. TRST is not the same signal as RESET)
3) See Section 1.5.1 for the recommended power and ground configuration.

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2.1 Pinout Package Arrangement (Top View)

	12	11	10	9	8	7	6	5	4	3	2	1	
M	AIN11	AIN14	AIN15	PCS	BOOTCFG [0]	UART0_RXD	UART0_TXD	CAN0_TXD	CAN0_RXD	SSN /GPIO43	MISO /GPIO42	MOSI /GPIO41	M
L	AIN10	AIN13	CLKSEL	VSSA	VDDA	TMS	TCK	Reserved	TDO	GPIO15	GPIO14	SCLK /GPIO40	L
K	AIN9	AIN12	RSTN	VSSA	VDDA	BOOTCFG [1]	Reserved	TDI	TRST	GPIO13	GPIO12	SDA1 /GPIO39	K
J	AIN8	AIN7	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO11	GPIO10	SCL1 /GPIO38	J
H	AIN3	AIN6	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO9	GPIO8	XTAL1	H
G	AIN2	AIN5	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO7	GPIO6	XTAL2	G
F	AIN1	AIN4	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO5	GPIO4	SDA0 /GPIO37	F
E	AIN0	Reserved	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO3	GPIO2	SCL0 /GPIO36	E
D	DAC0	CMP1+	LDO15_BYP	VSSA	VDDA	VSSA	VDDA	VDD	VSS	GPIO1	GPIO0	UART1_RXD /GPIO35	D
C	DAC1	CMP1-	LDO28_BYP	VSSA	VDDA	VSSA	VDDA	VSS	Reserved	PWM3 /GPIO47	PWM2 /GPIO46	UART1_TXD /GPIO34	C
B	CMP0+	Reserved	GPIO16 /INTR17	GPIO17 /INTR18	GPIO18 /INTR19	GPIO19 /INTR20	GPIO20 /INTR21	GPIO21 /INTR22	GPIO22 /INTR23	PWM1 /GPIO45	PWM0 /GPIO44	CAN1_TXD /GPIO33	B
A	CMP0-	GPIO24 /CMP0OUT	GPIO25 /CMP1OUT	GPIO26 /RTCK	GPIO27 /SSN1	GPIO28 /SSN2	GPIO29	GPIO30	GPIO31	GPIO23 /INTR24	CAN1_RXD /GPIO32		A
	12	11	10	9	8	7	6	5	4	3	2	1	

3 Absolute Maximum Ratings (1,2)

Table 7: Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
V_{DD}	Positive Digital Supply Voltage	-0.3	+4.2	V
V_{DDA}	Positive Analog Supply Voltage	-0.3	+4.2	V
P_D	Max Power Dissipation (3)	---	4.5	W
T_J	Junction Temperature	-55	+150	°C
θ_{JC}	Thermal resistance, junction-to-case	---	10	°C/W
T_{STG}	Storage Temperature	-65	+150	°C
ESD_{HBM}	ESD Protection (4)	---	2000	V
V_{ID}	Digital Pin Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
V_{IA}	Analog Pin Input Voltage	V_{SSA} - 0.3	V_{DDA} + 0.3	V

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) All V_{DD} voltages referenced to V_{SS} and all V_{DDA} voltages referenced to V_{SSA}.
3) Per MIL-STD-883, method 1012.1, section 3.4.1, $P_D=[T_J(max)-T_C(max))/\theta_{JC}]$. Using T_C = 105°C.
4) Per MIL-STD-883, method 3015.9, Table 3.

4 Operational Environment

Table 8: Operational Environment

Symbol	Parameter	Limit	Units
TID	Total Ionizing Dose (1, 2, 3)	50	krad(Si)
SEL	Single Event Latchup Immunity (4)	≤ 80	MeV-cm^2/mg
SER_{HI}	Heavy Ion Soft Error Rate (5, 6, 7)	≤ 8.30 × 10^{-8}	errors/device-day

Notes:

1) For devices procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
2) Per MIL-STD-883, method 1019.9, condition A.
3) For internal NOR Flash Memory Only. Irradiated per MIL-STD-883 Method 1019.9 Condition C at 50-300 rad(Si)/s using an in-situ 900 rad(Si) device unpowered and 100 rad(Si) device statistically biased duty cycle repeated 50 times to achieve a TID level of 50 krad(Si). This irradiation in-situ biasing method is predicated on an application which may allow the device to be unpowered during 90% of the mission life.
4) SEL characterization is performed at V_{DD} = V_{DDA} = 3.6 V and Tc ≥ 105°C. Contact factory for additional information.
5) SEU characterization is performed at V_{DD} = V_{DDA} = 3.0 V at 25°C. Contact factory for additional information.
6) The error rate calculation was performed using Adams 90% worst case environment, Geosynchronous Orbit, 100 mils Aluminum and applies to the internal SRAM.
7) Heavy Ion Soft-Reset Error Rate (SER) is defined as an erroneous output signal from the microcontroller device that can be corrected by performing one or more normal functions of the device. Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET.

5 Recommended Operating Conditions (1)

Table 9: Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Units
T_{OP}	Temperature Range	-55	+105	℃
T_C	Case Operating Temperature Range	-55	+105	℃
V_{DD}	Positive Digital Supply Voltage	+3.0	+3.6	V
V_{DDA}	Positive Analog Supply Voltage	+3.0	+3.6	V
V_{SS}	Digital Ground	+0.0		V
V_{SSA}	Analog Ground	+0.0		V

Note:

1) VDD referenced to VSS and VDDA referenced to VSSA.

6 General Electrical Characteristics

Unless otherwise noted, T_C is per the temperature range ordered.

For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

6.1 Test Conditions

6.1.1 Typical Values

The typical values are based on T_C = 25°C. V_{DD} = 3.3 V, and V_{DDA} = 3.3 V which are guaranteed by simulation and/or technology characterization unless otherwise specified. Typical values are for reference only and are not tested in production.

6.1.2 Minimum and Maximum Values

The minimum and maximum limits represent the test conditions based on supply voltages of V_{DD} = 3.3 V ± 0.3 V, V_{DDA} = 3.3 V ± 0.3 V, and temperature range of -55°C < T_C < +105°C by electrical test during production unless otherwise specified.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests.

Table 10. General Electrical Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
f_{SYSCLK}	System clock frequency		---	50	---	MHz
Q_{IDD}	V_{DD} supply current	All analog peripherals disabled, system clock off	---	---	6	mA
Q_{IDDA}	V_{DDA} supply current	All analog peripherals disabled	---	---	5	mA
A_{IDD}	V_{DD} active supply current	f_{SYSCLK} = 50 MHz	---	---	80	mA
A_{IDDA}	V_{DDA} active supply current	All analog peripherals enabled	---	---	20	mA

6.2 General Purpose I/O Characteristics

6.2.1 DC Characteristics (1)

Table 11: I/O DC Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
V_{IH}	High Level Input Voltage	$V_{OUT} \geq V_{OH(min)}$	2	---	V
V_{IL}	Low Level Input Voltage	$V_{OUT} \leq V_{OL(max)}$	---	0.8	V
I_{IH}	High Level Input Leakage Current	$V_{IN} = V_{DD}$	---	1	µA
I_{IL}	Low Level Input Leakage Current	V_{IN} = 0V	-1	---	µA
C_{IO}	Input Capacitance (2)		---	15	pF
V_{OH}	High Level Output Voltage	V_{DD} = min, I_{OL} = -100 µA	V_{DD} – 0.2	---	V
		V_{DD} = min, I_{OH} = -8 mA	2.4	---	
V_{OL}	Low Level Output Voltage	V_{DD} = min, I_{OL} = 100 µA	---	0.2	V
		V_{DD} = min, I_{OL} = 8 mA	---	0.4	
I_{OS}	Output short circuit current (3)	V_{OUT} = 0V or $V_{OUT} = V_{DD}$	-70	+70	mA
I_{INPU}	Input leakage; pull-up state	V_{IN} = 0V	10	65	µA
I_{INPD}	Input leakage; pull-down state	$V_{IN} = V_{DD}$	-65	-10	µA
I_{IHA}	Analog High Level Input Leakage Current (4)	V_{IN} = 2.9V	---	60	µA
I_{IH_DAC}	High Level Input Leakage Current for DACx (5)	$V_{IN} = V_{DD}$	---	35	µA
I_{IL_DAC}	Analog Low Level Input Leakage Current for DACx (5)	V_{IN} = 0V	-10	---	µA

Notes:

1) All voltages referenced to V_{SS}.
2) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
3) Guaranteed by design, not production tested.
4) Refers to AIN14 and AIN15 pins only.
5) Refer to DACx pins only.

6.2.2 AC Characteristics (1)

Table 12: I/O AC Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
t_r	Rise time		---	5	ns
t_f	Fall time		---	5	ns

Note:

1) Guaranteed by design, not production tested.

6.3 I²C PIN Characteristics (1,2,3)

Table 13: I²C I/O Characteristics

Symbol	Parameter	Conditions	Standard-Mode		Fast-Mode (15)		Fast-Mode Plus (15)		Units
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage		0.7*V_{DD}	---	0.7*V_{DD}	---	0.7*V_{DD}	---	V
V_{IL}	Low Level Input Voltage		-0.5	0.3*V_{DD}	-0.5	0.3*V_{DD}	-0.5	0.3*V_{DD}	V
I_{IH}	Input Leakage Current	0.1*V_{DD} < V_{IN} < 0.9*$V_{DD(max)}$	-10	+10	-10	+10	-10	+10	µA
C_{IO}	Input Capacitance (5)		---	10	---	10	---	10	pF
V_{OL}	Low Level Output Voltage (4)	V_{DD} > 2 V, I_{OL} = 3 mA (open-drain)	0	0.4	0	0.4	0	0.4	V
I_{OL}	Low Level Output Current (4)	V_{OL} = 0.4 V	3	---	3	---	20	---	mA
		V_{OL} = 0.6 V	---	---	6	---	---	---	mA
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ (4)		---	250	---	---	---	---	ns
f_{SCL}	SCL clock frequency (4)		0	100	0	400	0	1000	kHz
t_r	Rise time (4)	For both SDC and SCL signals	---	1000	20	300	---	120	ns
t_f	Fall time (4, 7, 8, 9, 10)	For both SDC and SCL signals	---	300	20+0.1 x Cb	300	---	120	ns
t_{LOW}	Low period of the SCL clock (4)		4.7	---	1.3	---	0.5	---	µs
t_{HIGH}	High period of SCL clock (4)		4.0	---	0.6	---	0.26	---	µs
$t_{SU;STA}$	Setup time for a repeated START condition (4)		4.7	---	0.6	---	0.26	---	µs
$t_{HD;DAT}$	Data hold time (4,11)		0	---	0	---	0	---	µs
$t_{SU;DAT}$	Data setup time (4)		250	---	100	---	50	---	µs
$t_{SU:STO}$	Setup time for STOP condition (4)		4.0	---	0.6	---	0.26	---	µs
t_{BUF}	Bus free time between a STOP and START condition (4)		4.7	---	1.3	---	0.5	---	µs
$t_{VD;DAT}$	Data valid time (4,12,13)		---	3.45	---	0.9	---	0.45	µs
$t_{VD;ACK}$	Data valid time (4,13,14)		---	3.45	---	0.9	---	0.45	µs

Notes:

1) All voltages referenced to V_{SS}.
2) See the I2C-Bus specification UM10204 for details.
3) All related AC (timing) related parameters tested with a load capacitance of 50 pf.
4) Guaranteed by design, not production tested.
5) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
6) Guaranteed by characterization.
7) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
8) Cb = total capacitance of one bus line in pF. Max of 400 pF in Standard- and Fast-Modes, and 550 pF in Fast-Plus Mode.
9) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
10) In Fast-Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
11) $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
12) $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
13) The $t_{HD;DAT}$ could be 3.45 us and 0.9 us for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
14) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
15) Compatible with Fast Mode and Fast Mode Plus specifications.

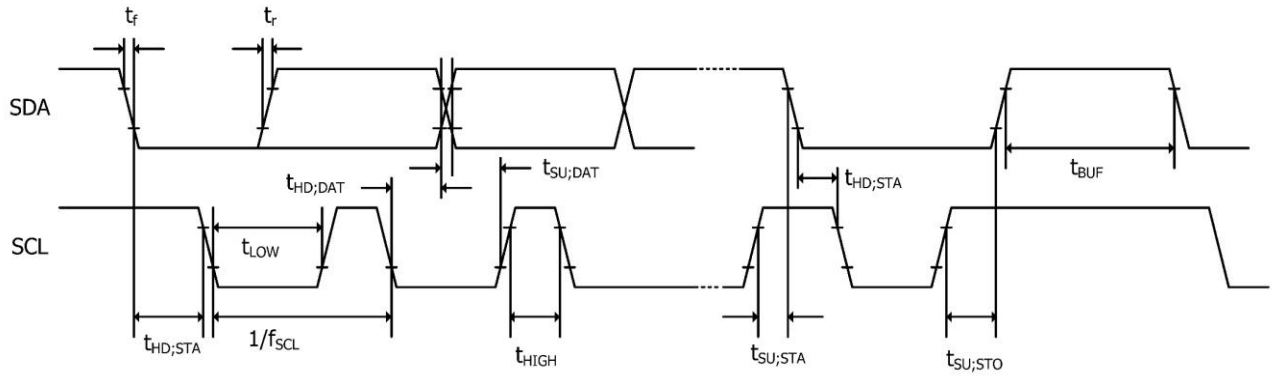

Figure 3: Timing definition for F/S mode of operation for I2C bus

6.4 SPI Characteristics

Table 14: SPI I/O Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
f_{SCK} (1)	SPI Clock frequency		---	10	MHz
t_{SCK} (1)	SPI Clock period		100	---	ns
t_H (1)	SCK High Time		50	---	ns
t_L (1)	SCK Low Time		50	---	ns
t_r (2)	SCK Rise time		---	25	ns
t_f (2)	SCK Fall Time		---	25	ns
t_{DS} (1)	Data input setup time wrt SCK edge		30	---	ns
t_{DH} (1)	Data input hold time wrt SCK edge		30	---	ns
t_{VD} (1)	Data out valid after SCK edge		---	30	ns
t_{DR} (2)	Data out rise time		---	30	ns
t_{DF} (2)	Data out fall time		---	30	ns
t_{HD} (1)	Data out hold time after SCK edge		5	---	ns
$t_{SU(SSN)}$ (1)	SSN low to first SCK edge		1 SCK Period		ns

Notes:

1) Guaranteed by design, not production tested.
2) Provided as a design limit only, neither production tested or guaranteed.

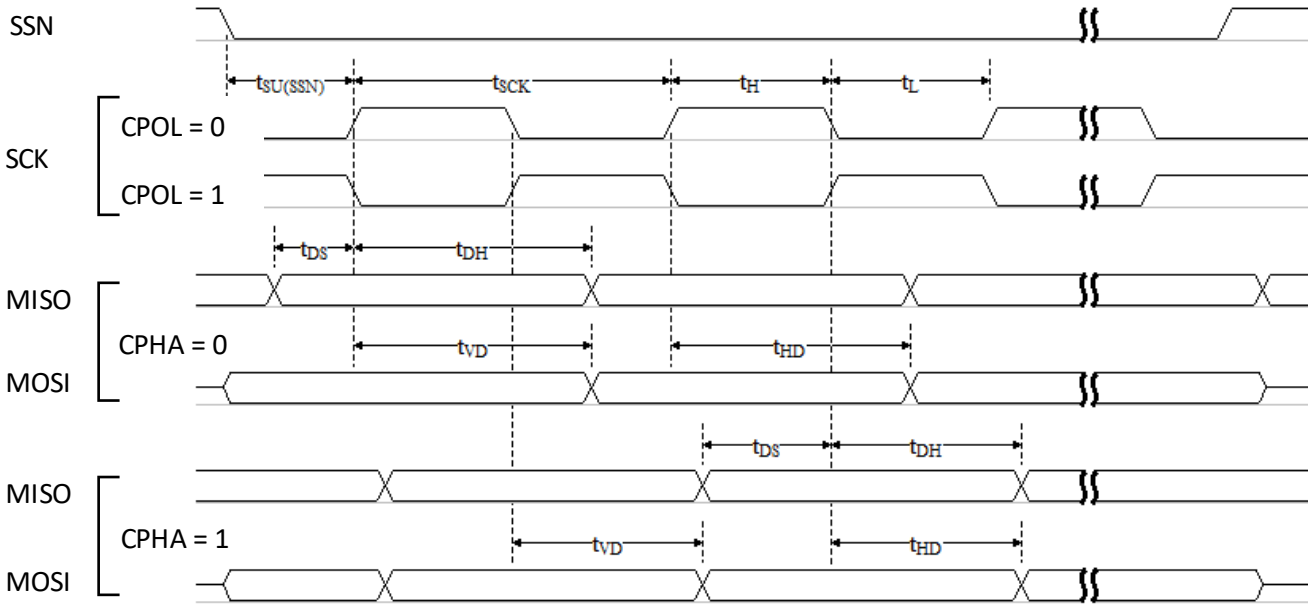

Figure 4: SPI Timing Diagram (Master Mode)

6.5 Oscillator Characteristics

6.5.1 Internal Clock Source Characteristics

Table 15: Internal Clock Source Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
f_{SYSCLK}	Frequency (1)	Typical = 50 MHz	---	52	MHz
	Duty Cycle (2)		40	60	%
	Accuracy	Factory Trimmed	-4	+4	%
	Internal Oscillator Startup (3)		---	6	μs

Notes:

1) Min value based on divider setting. See User manual for details
2) Guaranteed by characterization.
3) Provided as a design limit only, neither production tested or guaranteed.

6.5.2 External Clock Source Characteristics (1)

Table 16: External Clock Source Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
f_{XCLK}	Frequency (2)	Typical = 50 MHz	---	52	MHz
	Duty Cycle (2)	Typical = 50%	40	60	%
	External Clock input high level voltage	XTA L2 only	2	---	V
	External Clock input low level voltage	XTA L2 only	---	0.8	V

Notes:

1) All voltages referenced to V_{SS}.
2) Guaranteed by design, not production tested.

6.5.3 External Crystal Oscillator Characteristics

Table 17: External Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
f_{XOSC}	Crystal Frequency (1)		---	50	MHz
G_m	Maximum crystal transconductance (2)		---	80	mA/V
C_{XOSCL}	Supported crystal external load range (3)		8	16	pF

Notes:

1) Guaranteed by characterization using Statek CX1HGSM crystal.
2) Guaranteed by design, not production tested.
3) Provided as a design limit only, neither production tested or guaranteed.

6.6 12-Bit ADC Characteristics (Includes Analog Mux, PGA and AAF)

Table 18: 12-Bit ADC Characteristics

Symbol	Parameter	Conditions		MIN	TYP	MAX	Units
	Number of Channels (1, 2)	Single-ended Input			16		
		Differential Input			8		
Nbits	Resolution (1, 2)				12		bits
fADCK	Modulator Conversion Clock Frequency (1, 2)			---	---	12.5	MHz
INLADC	Integral Nonlinearity (1, 2)	PGA Gain = 1	Differential Input	-4	---	4	LSB
			Single-Ended Input	-4	---	22	
DNLADC	Differential Nonlinearity (1, 2)	PGA Gain = 1	Differential Input	-1.5	---	1.5	LSB
			Single-Ended Input	-1.2	---	2.0	
EOFF	Offset Error (1, 2)	PGA Gain = 1	Differential Input	-50	---	50	LSB
			Single-Ended Input	-50	---	50	LSB
GEADC	Gain Error (1, 2)	PGA Gain = 1		-4	---	1	% FSR
TCOFF	Offset Temperature Coefficient (3)			---	---	15	ppm/°C
SNR	Signal-to-Noise Ratio (1)	PGA Gain = 1,-3 dBFS, FIN =1 kHz sine wave	Differential Input	68	70	---	dB
			Single-Ended Input	58	60	---	
THD	Total Harmonic Distortion (3)	PGA Gain = 1, -3 dBFS, FIN = 1 kHz sine wave		---	-70	-65	dB
tCONV	Conversion Time (3,4)	Single-Shot Mode or Auto-Sequence (from start of convert command)		---	125	---	ADCK Cycles
	Initiation Time (3, 4, 5)	After ADC enable, PGA Gain = 1		---	1250	---	ADCK Cycles
ENOB	Effective Number of Bits (1)	10kHz sine wave, PGA Gain = 1	Differential Input	10	11	---	bits
			Single-Ended Input	9	9.5	---	
	Input Signal Range (1, 2, 6)	Single-ended input, PGA Gain = 1		0	---	1.5	V p-p
		Differential input, PGA Gain = 1, Vcm = 1.0 V		---	±1.5	---	

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
	Supply Current (3, 7)	Full signal path	---	---	14	mA
	Power Supply Rejection (1)	DC	46	---	48	dB
	Common Mode Rejection (3)	DC; Only applies to differential input signals	60	---	---	dB
	Input Common Mode Range (1)	Differential Input	0.4	---	1.4	V
Mux						
RSW	Switch On Resistance (3)	Gain = ½	---	267	300	kΩ
		1	---	200	---	
		2	---	133	---	
		4	---	80	---	
		8	---	44	---	
		16	---	24	---	
	Input Capacitance (3,8)	AINx pins only	---	---	16	pF
	Channel-to-Channel Crosstalk (1)	Differential input, Input Frequency=10 kHz	-70	---	---	dB
	Input Settling Time (3,9)	From input of mux to ADC to settle within 1/2 – LSB accuracy	12	20	28	µs
PGA and AAF						
	Programmable Gain Range (1,2,10)		0.5	---	16	V/V
	Filter Flatness (3)	Through 50 kHz baseband	---	±0.5	±1	dB
	Attenuation, Filter Stopband (3)	Input Frequency = 150 kHz	---	-3	---	dB
		600 kHz	---	-36	---	dB
		1.5 MHz	---	-60	---	dB
		6 MHz	---	-90	---	dB

Notes:

1) Guaranteed by characterization.
2) Functionally tested during production.
3) Guaranteed by design, not production tested.
4) Assumes clock for ADC (ADCK) = 12.5 MHz. See UT32M0R500 User Manual for details.
5) Initiation time is a time necessary for the ADC to achieve full accuracy. It is time after the ADC and PGA are enabled (power up) and a PGA gain is selected. This includes the multiplexer settling time.
6) Single-ended input is referenced to V_{SSA}.
7) Highest power supply current dissipation is at highest temperature, highest voltage.
8) Measured only for initial qualification and after process or design changes that could affect input/output capacitance. Includes capacitance from I/O.
9) Settling time is the time required from when an analog input is selected at the AMUX, which will settle to 12-bit accuracy, until the CONVERT command should be received by the ADC to begin a conversion operation.
10) Gain range has discrete levels of 0.5, 1, 2, 4, 8, and 16.

6.7 12-Bit DAC Characteristics (1)

Table 19: 12-Bit DAC Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
Static Performance						
N_{bits}	Resolution (3, 4)			12		bits
V_{REF_DAC}	Reference Voltage (2)		---	2.4	---	V
	Update rate (2)		---	---	100	kHz
INL_{DAC}	Integral Nonlinearity (3, 4, 5)		-4	±0.7	4	LSB
DNL_{DAC}	Differential Nonlinearity (3, 4, 5)		-3	±0.4	3	LSB
G_{E_DAC}	Gain Error (3)		-2.5	±0.2	2.5	%FSR
$\Delta G_{E\_DAC}/°C$	Gain Error Drift (2)		---	-3	---	ppm/°C
V_{OS}	Offset Error (3)	Code = 0x014	-50	---	50	LSB
$\Delta V_{OS}/°C$	Offset Error Drift (2)		---	8	20	ppm/°C
$ROUT_{sh}$	Output Impedance in Shutdown Mode (2)		---	100	200	kΩ
PSRR+	Supply rejection ratio (3)	Static DC measurement	37	---	43	dB
		No External Output Filter	---	250	---	μV rms
O_{Noise}	Output Noise (2)	With external 10 kHz Output Filter	---	128	---	
		With external 100 kHz Output Filter	---	41	---	
Dynamic Performance						
SR	Voltage Output Slew Rate (3)	Load = 5 kΩ//40 pF	---	---	1	V/μs
t_S	Output settling time to ½ LSB (2,6)	Load = 5 kΩ//40 pF	---	10	---	μs
V_{DAC_OUT}	Output voltage swing (3,4)	Load = 5 kΩ//40 pF	0	---	VREF – 1LSB	V
t_{ST}	Startup time (2)	From EN pin transitions low-to-high to valid VOUT value	---	10	---	μs
C_L	Max capacitance load for stability (2)	With or without RL = 5 KΩ	---	---	40	pF
Power Dissipation (each DAC)						
I_{ADAC}	Analog Supply Current (2)	Code = 0xFFF, Load =5 kΩ//40 pF	1.4	1.45	1.5	mA
I_{DDAC}	Digital Supply Current (2)	Frequency=100 kHz with updates to DAC0 and DAC1 data registers	---	---	1.5	mA
I_{SHDN}	Analog + Digital Supply Current during Shutdown (2)		---	35	300	nA
I_{SCDAC}	Output Short Circuit Current (2)	DACx shorted to either AVDD or AVSS	---	15	22	mA

Notes:

1) All voltages referenced to V_{SSA}.
2) Guaranteed by design, not production tested.
3) Guaranteed by characterization (using input codes 21 – 4095 for INL and DNL).
4) Functionally tested during production.
5) ±1LSB = ±0.0244% of Full Scale = ±244 ppm. Full Scale = 2.4V.
6) Settling time with change from code 0xFFF to 0x014. Time measured from rising edge of data word to within ±0.5LSB of final value with a load = 40 pF.

6.8 Comparator Characteristics (1)

Table 20: Comparator Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{CMR}	Input Common-Mode Voltage Range (2)		0.0	---	V_{DDA}	V
V_{HYS}	Input-Referred Hysteresis (2, 3)	$V_{CM} = V_{DDA}$	15	35	110	mV
		$V_{CM} = V_{DDA}/2$	5	20	35	mV
		$V_{CM} = 0V$	8	14	25	mV
V_{TRIP+}	Input-Referred Positive Trip Point (2, 3, 4)	$V_{CM} = V_{DDA}$	2	---	52	mV
		$V_{CM} = V_{DDA}/2$	1	---	20	
		$V_{CM} = 0V$	4	---	11	
V_{TRIP-}	Input-Referred Negative Trip Point (2 ,3, 4)	$V_{CM} = V_{DDA}$	-2	---	-52	mV
		$V_{CM} = V_{DDA}/2$	-1	---	-20	
		$V_{CM} = 0V$	-4	---	-11	
V_{OS}	Input Offset Voltage (2, 5)	V_{CM} = 0V, or $V_{CM} = V_{DDA}/2$, or $V_{CM} = V_{DDA}$	0	---	10	mV
CMRR	Common-Mode Rejection Ratio (2 ,7)	V_{DDA} = 3.3V , V_{CM} = -0.1V and 3.4V	---	1.5	4	mV/V
PSRR	Power-Supply Rejection Ratio (2, 8)	$V_{CM} = V_{DDA}/2$	---	1	2	mV/V
t_{PD}	Propagation Delay (6, 9)	Overdrive = 10 mV	55	80	110	ns
t_{SKEW}	Propagation-Delay Skew (2, 10)	Overdrive = 10 mV	-100	---	100	ns

Notes:

1) All voltages referenced to V_{SSA}.
2) Guaranteed by characterization, not production tested.
3) The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis.
4) The input-referred trip points are the limits of the differential input voltage (for Vcm = 0.0) required to make the comparator output change state.
5) The Input Offset Voltage is defined as the mean of the trip points. $V_{OS} = (V_{TRIP+} - V_{TRIP-})/2$.
6) Guaranteed by design, not production tested.
7) CMRR = $(V_{OSL}-V_{OSH})$ / 3.6V, where V_{OSL} is the offset at V_{CM} = -0.1V and V_{OSH} is the offset at V_{CM} = 3.4V.
8) PSRR = $(V_{OS3} - V_{OS3.6})$ / 0.6V where V_{OS3} is the offset voltage with V_{DDA}=3V, and $V_{OS3.6}$ is the offset voltage with V_{DDA} = 3.6V.
9) Functionally tested during production.
10) Propagation Delay Skew is the difference between t_{PDLH} and t_{PDHL}.

6.9 Pulse Width Modulator Characteristics (1)

Table 21: PWM Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
	Maximum period count	16-bit	2	65,535	Counts
	Dead band Range		20	81,920	Counts
	Clock Prescalar Range		1	256	Counts

Note:

1) Guaranteed by design, not production tested.

6.10 Timer Characteristics (1, 2)

Table 22: Timer/Counter Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
	Maximum possible count	32-bit register	---	4.3E9	Count

Notes:

1) Functionally tested during production.
2) Guaranteed by design, not production tested.

6.11 UART Characteristics (1, 2, 3)

Table 23: UART Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
	Baud rate		600	115,200	Bd/s

Notes:

1) Provided as a design guideline, not production tested or guaranteed.
2) Functionally tested during production.
3) Guaranteed by design, not production tested.

6.12 Power-on-Reset Characteristics (1, 2)

Table 24: Power-On-Reset Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
t_{RD}	Reset Delay Time		16	128	ms
V_{DD_RTH}	V_{DD} Threshold Range	During power-up only	1.30	2.60	V
V_{DDA_RTH}	V_{DDA} Threshold Range	During power-up only	1.30	2.60	V

Notes:

1) All voltages referenced to V_{SS}.
2) Guaranteed by design, not production tested.

6.13 Temperature Monitor (1, 2, 3)

Table 25: Temperature Monitor Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
	Nonlinearity		-4	---	5	°C
	Absolute Accuracy		---	---	12	°C
	Gain		-3.2	---	---	mV/°C
	Offset	Temp = 0 °C	-1.2	---	---	V
	Active Current Consumption (4)		68	---	103	μA

Notes:

1) Functionally tested during production.
2) Guaranteed by characterization, not production tested.
3) PGA gain at 16x.
4) Provided as a design guideline, not production tested or guaranteed.

6.14 Precision Current Source

Table 26: Precision Current Source Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
I_{out}	Source Current(1)		---	1	---	mA
	Current Precision	Typ = 1.0 mA +25°C	-1.5	---	1.5	%FS
	Current Drift Over Temperature	-55°C to +105°C	-5.0	---	5.0	%FS
$t_{EDILH(1)}$	Enable delay to Iout(1)		---	---	100	ns

Note:

1) Guaranteed by design, not production tested.

7 Memory Characteristics

7.1 NOR Flash Memory

Table 27: Endurance and Retention for the NOR Flash Memory as used.

Parameter	Conditions	Limit	Units
Minimum data retention (1)	TC = 105°C	5	Years
	TC = 90°C	21	
	TC = 75°C	85	
	TC = 60°C	350	
Minimum endurance	TC = -40°C to 105°C	10k	Cycles per sector

Note:

1) Data retention table is predicted on initial user programmed cycle of the device.

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8 Packaging

8.1 143-Pin CLGA Package Outline Drawing

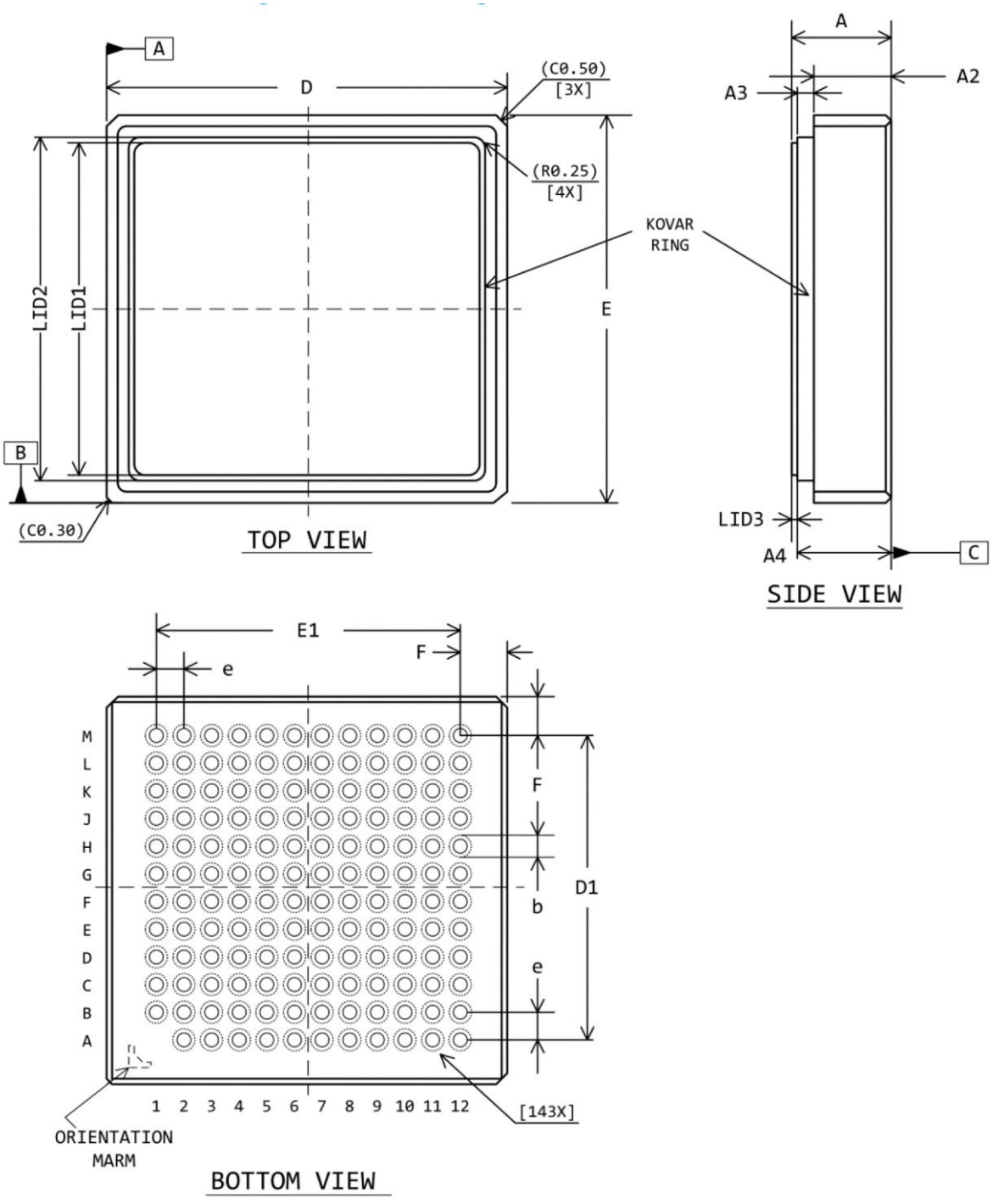

Figure 5: 143-Lead Ceramic Land Grid Array (CLGA)

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Symbol	Millimeters		
	MIN	TYP	MAX
A			5.28
A2	3.6	4.0	4.4
A3	0.60	0.65	0.70
A4	4.20	4.65	5.10
b	0.75	0.80	0.85
D/E	14.35	14.5	14.65
D1/E1	10.87	11.0	11.13
e	0.95	1.0	1.05
F		1.75	
LID1	12.38	12.43	12.47
LID2	12.81	12.94	13.07
LID3	0.124	0.127	0.130

Notes:

1) Material is 90%-minimum alumina (er = 9.8)
2) Units are millimetres
3) Lid is connected to VSS
4) Exposed-metal plating per MIL-PRF-38535
   - Nickel base: electro-plated 2.54 – 8.89um
   - Gold: Electro-plated 2.54 – 5.72um

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8.2 143-Pin CCGA Package Outline Drawing

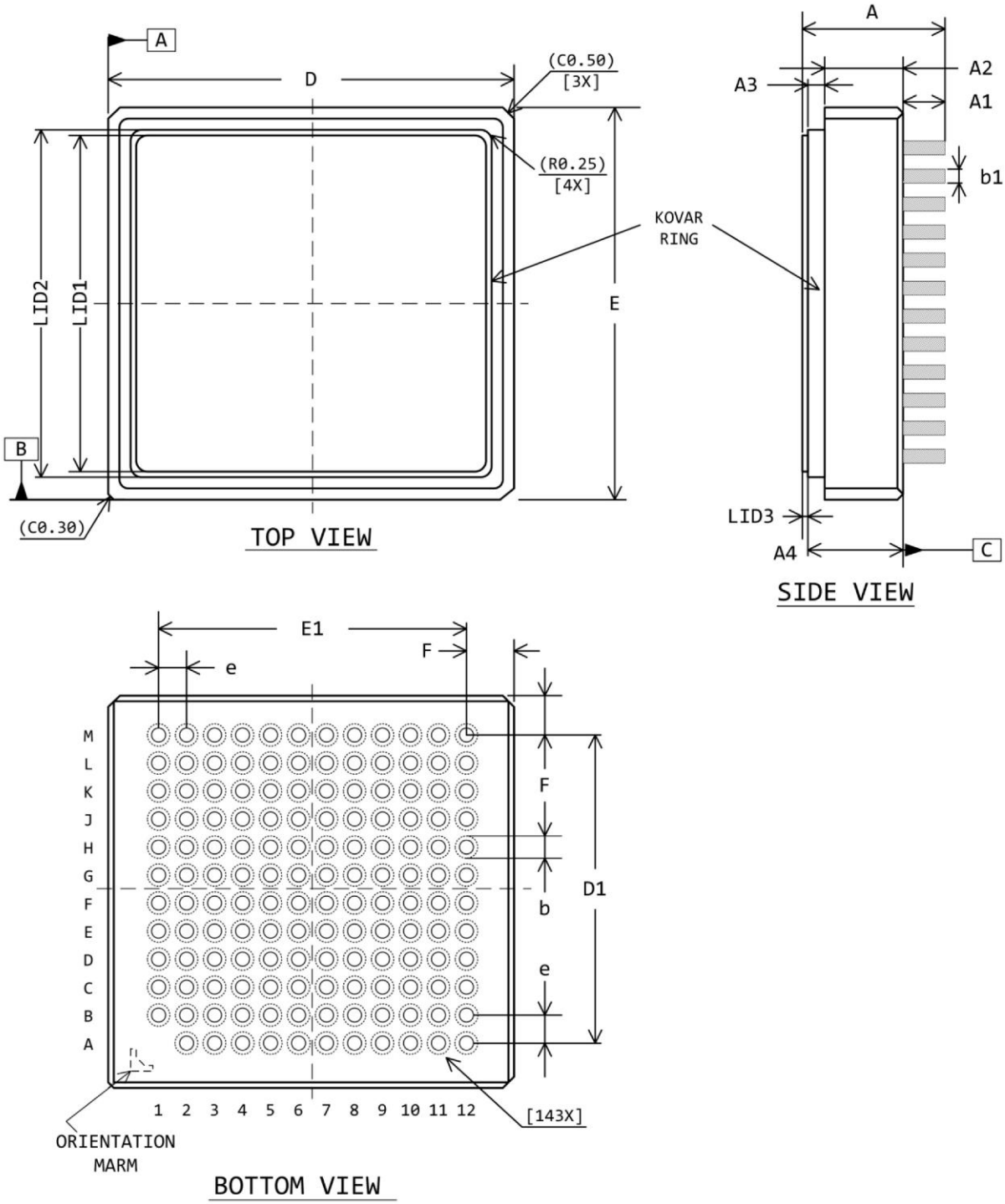

Figure 6: 143-Lead Ceramic Column Grid Array (CCGA)

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Symbol	Millimeters		
	MIN	TYP	MAX
A			7.69
A1	2.01	2.21	2.41
A2	3.6	4.0	4.4
A3	0.60	0.65	0.70
A4	4.20	4.65	5.10
b	0.75	0.80	0.85
b1	0.51	0.51	0.61
D/E	14.35	14.5	14.65
D1/E1	10.87	11.0	11.13
e	0.95	1.0	1.05
F		1.75	
LID1	12.38	12.43	12.47
LID2	12.81	12.94	13.07
LID3	0.124	0.127	0.130

Notes:

1) Material is 90%-minimum alumina (er = 9.8)
2) Units are millimetres
3) Lid is connected to VSS
4) Exposed-metal plating per MIL-PRF-38535
   - Nickel base: Electro-plated 2.54 – 8.89um
   - Gold: Electro-plated 2.54 – 5.72um

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8.3 143-Pin CBGA Package Outline Drawing (Prototype Only)

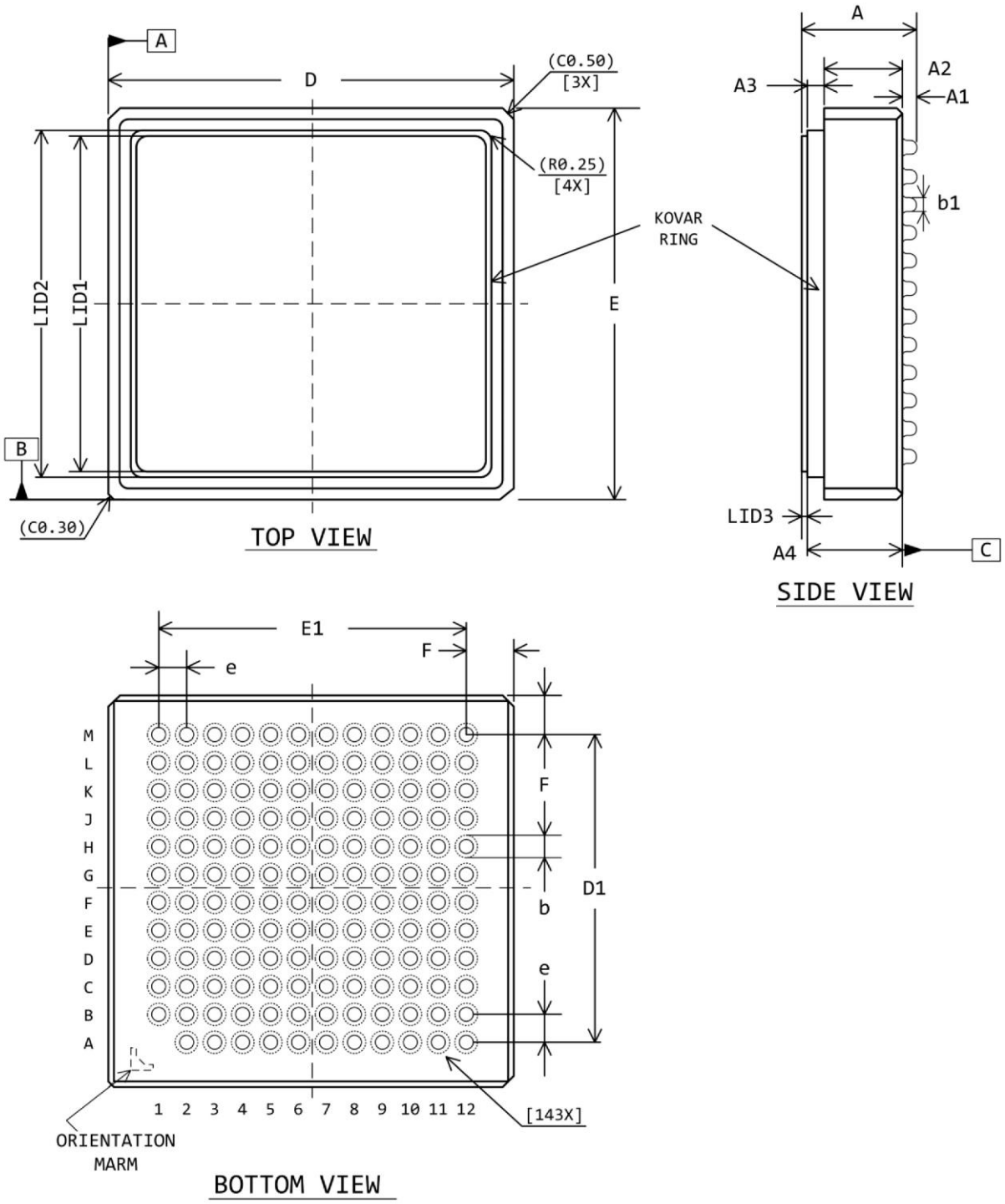

Figure 7: 143-Lead Ceramic Ball Grid Array (CBGA)

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Symbol	Millimeters		
	MIN	TYP	MAX
A			5.96
A1	0.50	0.60	0.70
A2	3.6	4.0	4.4
A3	0.60	0.65	0.70
A4	4.20	4.65	5.10
b	0.75	0.80	0.85
b1	0.50	0.60	0.70
D/E	14.35	14.5	14.65
D1/E1	10.87	11.0	11.13
e	0.95	1.0	1.05
F		1.75	
LID1	12.38	12.43	12.48
LID2	12.81	12.94	13.07
LID3	0.097	0.127	0.157

Notes:

1) Material is 90%-minimum alumina (er = 9.8)
2) Units are millimetres
3) Lid is connected to VSS
4) Exposed-metal plating per MIL-PRF-38535
   - Nickel base: electro-plated 2.54 – 8.89um
   - Gold: electro-plated 2.54 – 5.72um

8.4 143-Pin PBGA Package Outline Drawing (Preliminary, see Datasheet Definitions)

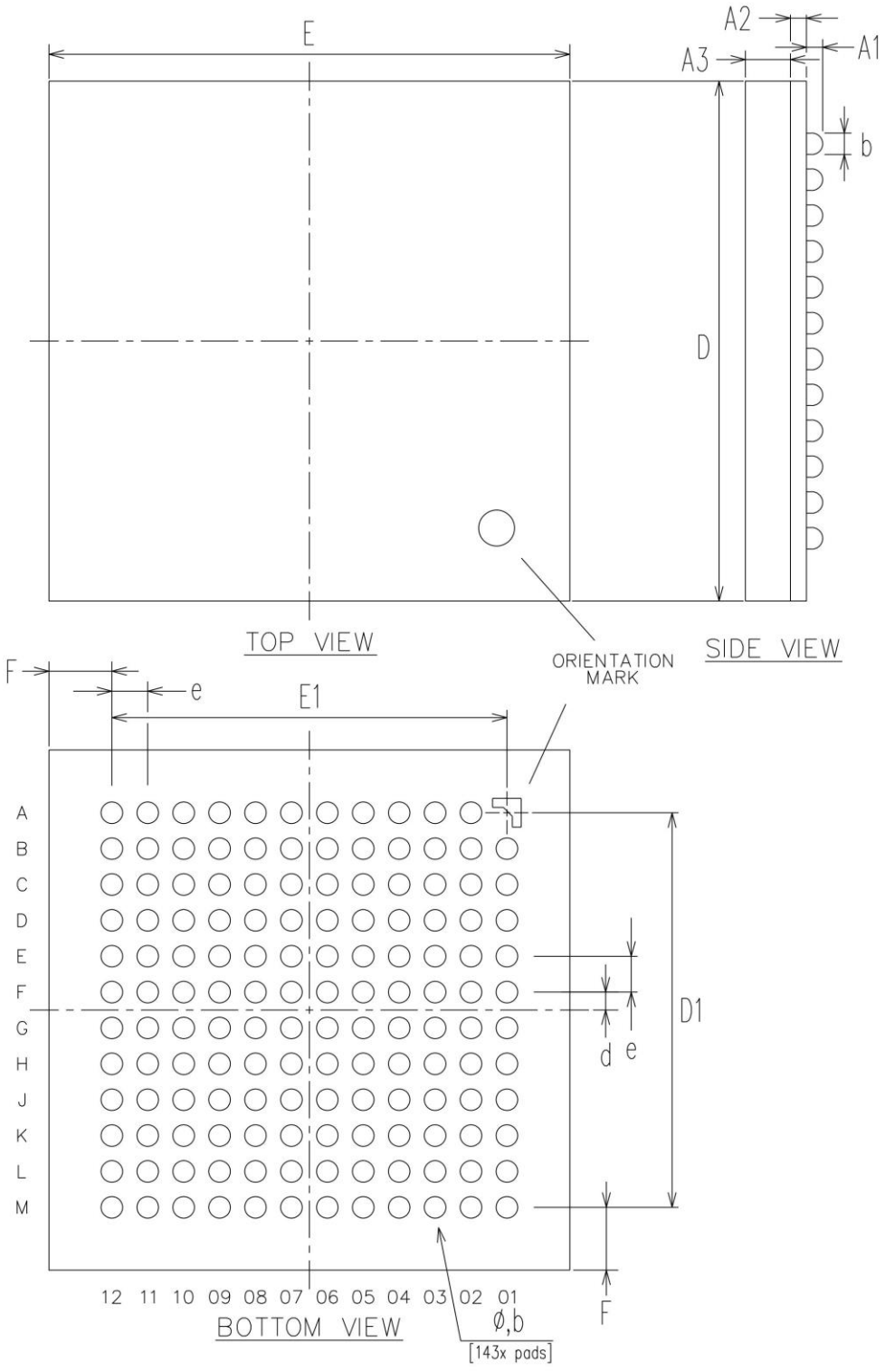

Figure 8: 143-Lead Plastic Ball Grid Array (PBGA)

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Symbol	Millimeters		
	MIN	TYP	MAX
A1	0.35	0.45	0.55
A2	0.40	0.45	0.50
A3		1.25	
b	0.55	0.60	0.65
D/E	14.35	14.5	14.65
D1/E1	10.87	11.0	11.13
d		0.50	
e	0.95	1.0	1.05
F		1.75	

Notes:

1) Substrate Material is HL832NS
2) Substrate is Overmolded
3) Solder Balls are 0.6mm 63Sn/37Pb Eutectic
4) LGA Pad metal is 0.5mm Diameter
5) Soldermask Opening is 0.6mm Diameter

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9 Ordering Information

9.1 CAES Part Number Ordering Information

Generic Datasheet Part Numbering

UTxxxxx * * * *

Lead Finish: (Notes: 1)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Screening Level: (Notes: 2, 3, 4, 5, and 6)
(P) = Prototype Flow (Temperature Range: 25°C only)
(F) = HiRel Flow (Temperature Range: -55°C to +105°C)
(L) = Constellation Flow (Temperature Range: -55°C to +105°C)
(N) = Constellation Flow (Temperature Range: -55°C to +105°C)

Case Outline: (Note: 7)
(Z) = 143-Ceramic Land Grid Array
(S) = 143-Ceramic Column Grid Array
(C) = 143-Ceramic Ball Grid Array
(B) = 143-Plastic Ball Grid Array

Radiation Hardness Assurance: (Note: 8)
(-) = No Radiation Assurance
(L) = 50 krad(Si)

Device Type:
(500) = 50MHz Operating Frequency

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Notes:

1) Lead finish (A, C or F) must be specified
2) Prototype Flow per CAES Manufacturing Flows Document. Radiation is neither tested nor guaranteed
3) HiRel Flow per CAES Manufacturing Flows Document. Radiation TID tolerance may not be ordered
4) Constellation Flow Per CAES Manufacturing Flows Document. Available in Ceramic Land Grid Array (CLGA), Ceramic Column Grid Array (CCGA), and Plastic Ball Grid Array (PBGA) packages. Use screening flow character "L" for ceramic packages, and "N" for plastic packages.
5) For Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) packages, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column)
6) Contact factory to define alternative screening options
7) Ceramic Ball Grid Array leads are only available for Prototype Screening Level
8) 50krad radiation tolerance only available for the "L" Constellation Flow with an "S" 143-Ceramic Column Grid Array case or the "N" Constellation Flow with a "B" 143-Plastic Ball Grid Array case

9.2 SMD Part Number Ordering Information

SMD Part Numbering

5962 * ***** ** * * *

Lead Finish: (Notes: 1)
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Case Outline: (Note: 2)
(X) = 143-lead Ceramic Land Grid Array
(Y) = 143-lead Ceramic Column Grid Array

QML/JAN Class: (Note: 3, 4)
(Q) = Class Q

Device Type:
(01) = UT32M0R500 (QML Q)
(02) = UT32M0R500 (QML Q+)

SMD Project Number:
(17212) = 32-Bit Microcontroller

Radiation Hardness Assurance:
(L) = 50 krad(Si)

Federal Stock Class Designator

Notes:

1) Lead finish (C or F) must be specified
2) For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) packages, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column)
3) Contact factory to determine alternative screening options
4) CAES Q+ flow, as defined in Section 4.2.1d of the SMD, provides QML-Q product through the SMD that is manufactured with CAES standard QML-V flow

10 Revision History

Date	Revision		Change Description
10/05/2017	1.0.0		Released Advanced Datasheet
12/2017	1.1.0		Released Preliminary Datasheet
02/2018	1.1.1		Modifications to comparator limits and notes for clarification
03/2018	1.2.2		Modified some comparator specifications to guaranteed by design; Include notes on tables 18 and 19.
04/2018	1.2.3		Reformatted the I/O table and added PU/PD column; Updated comparator notes; Added (F) option for Lead Finish on ordering page
07/2018	1.2.4		Removed Table 2.; Changed "Soft" to "Heavy Ion" in Table 8.; Added note on using Adams 90% WC to Table 8; Added general statement on TID in section 6.; Added note for Cin in Table 11; Change "characterization" to "design" for Table 13; Change note references in Table 13; Added reference crystal in Note 1 in Table 17; Changed "Power" to "Active Current Consumption" in Table 25; Modified the A , A4, and b1 parameters for the CLGA package; Modified the A4 and b1 parameters for the CCGA package.; Updated SER specification;
09/2018	1.2.5		Datasheet Release; Updated QIDDA specification; Updated the IINPU and IINPD limits; Added package outline drawing for C BGA; Updated the UT ordering page for correct placement of the '-';
11/2018	1.3.0		Updated QIDD, QIDDA; Added AIDD, AIDDA; Modified ADC INL, DNL, Offset, Gain Error; Modified DAC INL, DNL, Offset, Gain Error
11/2018	1.3.1		Added "Released Datasheet" to title page; Modified note on characterization for DAC2
11/2018	1.3.2		Moved to min to max column for the ADC THD parameter
01/16/19	1.3.3	JA	Date Update
02/04/19	1.3.4	MF	Parameters for CBGA package
02/07/19	1.3.5	OW,JA	Pin list Power on Reset Clarification
02/27/19	1.3.6	OW,JA	Modified Offset and Gain errors; deleted timer input capture statement
4/11/19	1.3.7	OW	Added JTAG recommendations; Changed pin C4 to Reserved; Added V_{ID} and V_{IA} to the Absolute Maximum Table
4/30/19	1.3.8	OW	Added *Lean*REL™ flow as an option
6/12/19	1.3.9	OW	Updated SMD ordering page to correctly list device types; Removed "Hysteresis of Schmitt Trigger Inputs" from I^2C I/O Characteristics Table 13
2/25/2021	2.0.0	OW	Corrected the Heavy Ion Soft Error Rate specification; Removed the LeanREL® section at the beginning of the datasheet; Updated SPI section to clarify bus connectivity, Tx and Rx FIFO size, and RX sample point delay description; Reserved "NFC AHB I/F" from Memory Map Table 4 to match Functional Manual; Revised Pinlist PU/PD column; Corrected Default State of GPIO[16:31] in the Pinlist table; Updated VIN conditions of the IIHA specification; Removed Input Leakage Current from ADC Characteristics (Use IIH, IIL, and IIHA from the DC Characteristics); Changed the Pinlist Table's column from Value During POR to Value Before POR to appropriately describe when this condition occurs; Added note 7 to table 8; Table 15 pointed to note 14 where it meant 15 and vice versa, corrected them; Updated SPI Specifications table to include tSU(SSN); Fixed the SPI Timing Diagram by correcting the MOSI/MISO labels, and removing labels

			without an associated specification; Updated Comparator V_{OS}, CMRR, and PSRR specs to specify guaranteed by characterization, not by design, and t_{PD} to specify by design, not by characterization; Updated Precision Current Source "Current Precision" to specify it is production tested at +25°C; Added the "Current Drift Over Temperature" specification to the PCS table; Updated CAES Part Ordering Information "L" Screening Level from *Lean*REL™ to EQM/Industrial Flow
5/10/2021	2.1.0	OW	Added the Plastic Ball Grid Array Package with "Preliminary" markings; Added PBGA drawing to datasheet; Updated part ordering information to include PBGA orders; Re-named EQM/Industrial Flow to Constellation Flow;
5/17/2022	2.1.1	OW	Added recommendation for split power and grounds to section 1.5.1, and note 3 to Table 6: Pinlist; Fixed SPI Timing Diagram to show MOSI Hi-Z state outside transactions;

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32-Bit Arm® Cortex®-M0+ Microcontroller

UT32M0R500

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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