DATASHEET

RELEASED 01/13/22

1.25 Gbps LVDS Repeater

UT54LVDS454

Features

- LVDS repeater
  - One part, two functions:
    - Full-duplex dual repeater
    - Simplex quad repeater
- Data Rates up to 1.25 Gbps per channel
- Protocol Independent
- Cold sparing all pins
- Low Propagation Delay
- Low Channel-to-Channel Skew
- Supports up to 1 meter of FR4 PCB or 10 meters of cable up to 1.25Gbps
- Single 2.5V +/-5% power supply
- Selectable 3.5mA or 7.0mA output drive currents
- Low power standby mode
- Enable/Enable* input to disable LVDS drivers
- Fail-safe function for loss of signal detection
- Compatible with TIA/EIA-644A LVDS standard
- QML V Qualification Pending
  - SMD # 5962-21211
- Package Information:
  - 71-Pin Ceramic Land Grid Array (C-LGA), Ball Grid Array (C-BGA), Column Grid Array (C-CGA) Options
  - Small QML package Size: 9.0 mm x 10 mm, 1 mm Pad Pitch

Operational Environment

- Temperature Range: -55°C ≤ Tc ≤ +105°C
- Total Dose: 100 kRad (Si)
- SEL Immune: ≤ 100 MeV-cm^2/mg

Applications

- High-Speed Dual LVDS Full-Duplex Repeater
- High-Speed Quad LVDS Simplex Repeater
- Mission Critical FPGA LVDS I/O Protection

Introduction

The UT54LVDS454 is a single high performance device that can be configured by pin connection through PCB high-speed signal layout as either a dual, full-duplex or a quad, simplex LVDS repeater. Both configurations are intended for high-speed, high-reliability, space, or other harsh environment serial link applications. See block diagrams as Figures 1.2 and 1.3, below.

The selectable TX drive current and back-termination resistor options allow the user optimize between power dissipation and signal integrity (SI). Coupled with the user-supplied external RX/TX differential 100Ω terminations, and small LGA package footprint, the UT54LVDS454 provides for maximum application flexibility in systems with mission critical serial link full redundancy requirements.

For short reach, e.g. ≤10cm, and/or lower data rates, up to approximately 600 Mbps, the TX drive current can be reduced by half to 3.5mA and the back-termination resistor not installed. This is the standard LVDS configuration and provides good SI and BER performance at low power consumption. For longer links, e.g. >10cm, and/or higher data rates, from approximately 600 Mbps to the maximum of 1.25 Gbps, the TX drive current can be

increased to 7.0mA along with installing the back-termination resistor for improved SI and BER performance at somewhat higher, but still low power consumption.

The cold-sparing all pins feature enables both primary and redundant devices to be installed on the same point-to-point channel at up to 400 Mpbs with good SI. Because of additional channel loading in this case due to both primary and redundant devices at the near-end TX transmitter and far-end RX receiver, system-level cold spare implementation at higher data rates may require dual point-to-point channels or other topologies to achieve acceptable SI and link BER.

1.0 Functional Description

Overview

Figure 1.1 illustrates the functionality of a single channel of the UT54LVDS454 LVDS Repeater. Figure 1.2 shows the device block diagram. The device is comprised of four independent LVDS channels, all of which are controlled by a common digital section.

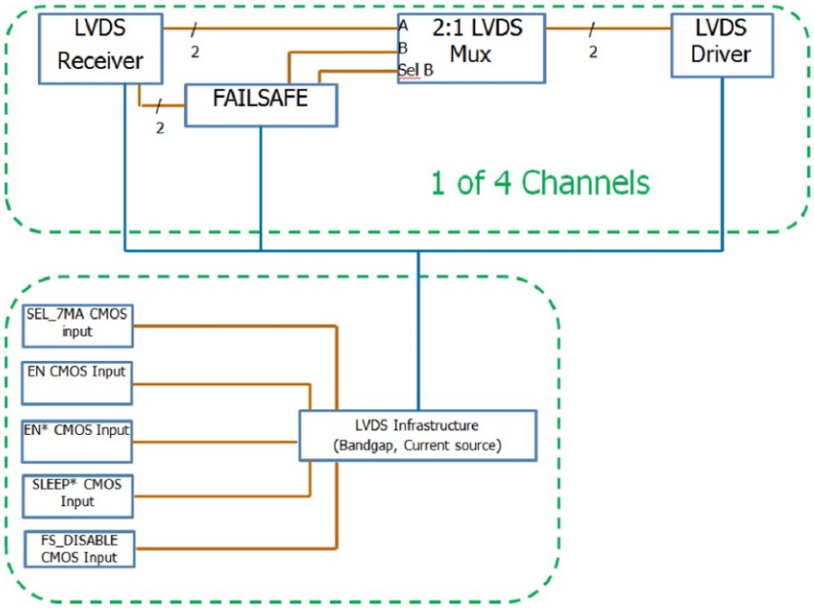

Figure 1.1: UT54LVDS454 Repeater Single Channel Functional Block Diagram

Table 1.1: Logic Function Truth Table

Mode	VDD	EN	EN*	SLEEP*	SEL_7MA	FS_DISABLE	Description
Normal Operation 3.5mA drive	2.5V	2.5V	0V	2.5V	0V	0V	Normal LVDS in to LVDS out. 3.5mA output drive. Limitation on low frequency operation.
						2.5V	Normal LVDS in to LVDS out. 3.5mA output drive. No limitation on low frequency operation.
Normal Operation 7mA drive	2.5V	2.5V	0V	2.5V	2.5V	0V	Normal LVDS in to LVDS out. 7mA output drive. Limitation on low frequency operation.
						2.5V	Normal LVDS in to LVDS out. 7mA output drive. No limitation on low frequency operation.
LVDS Outputs Disabled	2.5V	0V	X	2.5V	X	X	LVDS outputs floating.
		X	2.5V			X	
Sleep	2.5V	X	X	0V	X	X	Low power disable mode.
Cold Spare	0V	X	X	X	X	X	Cold spare mode. All I/O floating.

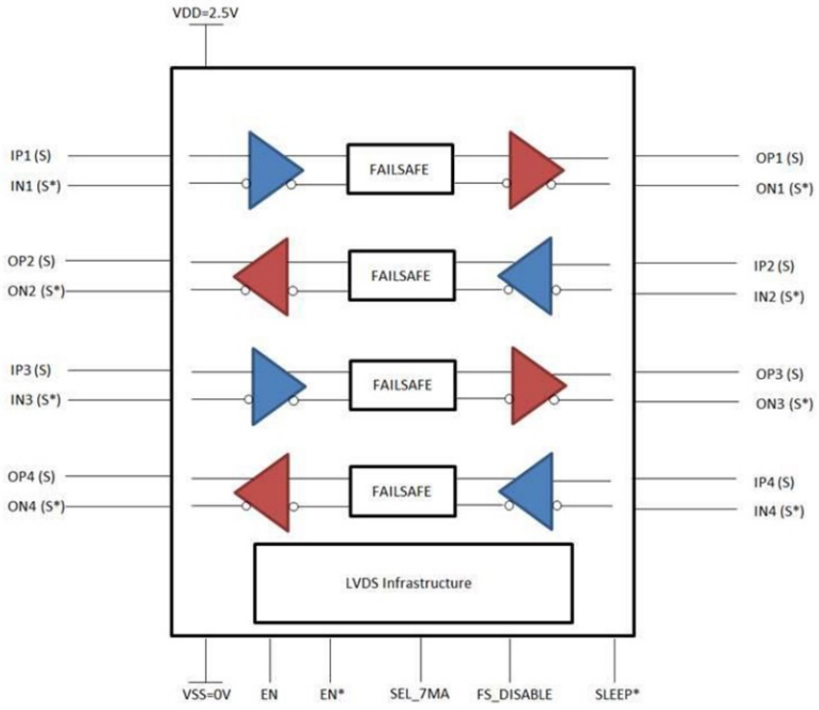

Figure 1.2: UT54LVDS454 Dual, Full-Duplex Repeater Block Diagram

1.25 Gbps LVDS Repeater

UT54LVDS454

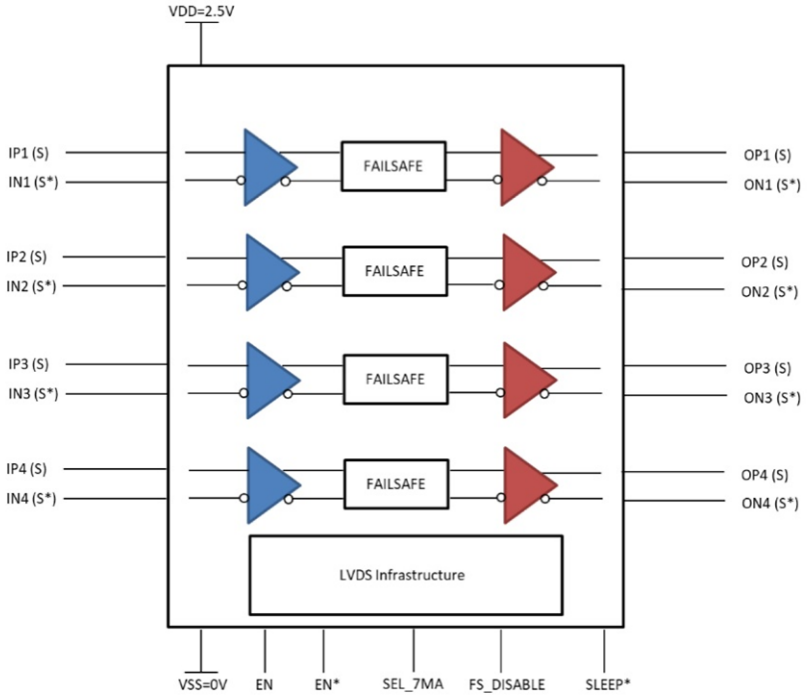

Figure 1.3: UT54LVDS454 Quad, Simplex Repeater Block Diagram

UT54LVDS454 Input Receiver

The UT54LVDS454 Receiver (RX) input buffers operate using the Low Voltage Differential Signaling (LVDS) I/O standard. The inputs must be externally terminated with 100Ω between the differential signals. The input buffers support an amplitude range of 100mVp-p to 2,500mVp-p differential voltage. The common-mode input range is 0.1V to VDD-0.1V, with a 150mV differential input around the common-mode input voltage. An input fail safe circuit detect function is implemented and activated with FS_DISABLE pin set to logic low. With the fail-safe function enabled, if an input signal edge rate falls below 1MHz rate, the respective LVDS output is driven to a logic 1 state.

UT54LVDS454 Output Driver

The UT54LVDS454 Output Driver (TX) operates using the Low Voltage Differential Signaling (LVDS) I/O standard. Each output must be terminated at the far-end RX in 100Ω for the 3.5mA drive option, or both at the near-end TX and the far-end RX for the 7mA drive option. The TX output differential amplitude range is 250 to 400mVp-p for either (a) 3.5mA, 100Ω load, or (b) 7.0mA, 50Ω load. The output common mode (offset) voltage (VOS) range is 1.25V-1.40V.

2.0 Device Pin Description

Input-Output and Control Pin Description

Table 2.1: UT54LVDS454 Input-Output and Control Pin Description

Pin Name	Description
IP#	Positive LVDS input. # associated with the channel corresponding to the input pin.
IN#	Negative LVDS input. # associated with the channel corresponding to the input pin.
OP#	Positive LVDS output. # associated with the channel corresponding to the output pin.
ON#	Negative LVDS output. # associated with the channel corresponding to the output pin.
SLEEP*	Active Low, Ultra-Low Power Sleep pin – LVCMOS Input.
EN	Active High Transmitter Enable – LVCMOS Input.
EN*	Active Low Transmitter Enable – LVCMOS Input.
SEL_7MA	Active High 7mA drive current select pin. 3.5mA when low – LVCMOS Input.
FS_DISABLE	Active High failsafe disable – LVCMOS Input.
VSS	Power Supply Ground Return. 0V.
VDD	Positive Power Supply, 2.5V nominal.

Table 2.2: UT54LVDS454 Package Pad Location and Function

Package Pad Location	Package Pad Name	Package Pad Function and Type
A01	<no pad>	Land #1 - No Connect (N/C)
LVDS Transmit (TX) Differential Signal Pairs		
G08	OP1	Positive LVDS channel 1, output
H08	ON1	Negative LVDS channel 1, output
J02	OP2	Positive LVDS channel 2, output
J03	ON2	Negative LVDS channel 2, output
A03	OP3	Positive LVDS channel 3, output
A02	ON3	Negative LVDS channel 3, output
B08	OP4	Positive LVDS channel 4, output
C08	ON4	Negative LVDS channel 4, output
LVDS Receive (RX) Differential Signal Pairs		
J06	IP1	Positive LVDS channel 1, input
J07	IN1	Negative LVDS channel 1, input
G01	IP2	Positive LVDS channel 2, input
H01	IN2	Negative LVDS channel 2, input
B01	IP3	Positive LVDS channel 3, input
C01	IN3	Negative LVDS channel 3, input
A06	IP4	Positive LVDS channel 4, input
A07	IN4	Negative LVDS channel 4, input

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Package Pad Location	Package Pad Name	Package Pad Function and Type
Control Signals		
C06	FS_DISABLE	Failsafe disable, input
D02	SLEEP*	Sleep function, input
E02	SEL_7MA	TX Output Drive select, input
F02	EN*	TX Output Enable, input
H04	EN	TX Output Enable, input
CAES-Only Signals		
B05	CAES USE ONLY	Connect R_{EXT}=20KΩ to VSS
Power		
B06	VDD	POWER
C04	VDD	POWER
C07	VDD	POWER
D03	VDD	POWER
D04	VDD	POWER
D05	VDD	POWER
E01	VDD	POWER
E03	VDD	POWER
E05	VDD	POWER
E06	VDD	POWER
E08	VDD	POWER
F03	VDD	POWER
F04	VDD	POWER
F06	VDD	POWER
G02	VDD	POWER
G03	VDD	POWER
G05	VDD	POWER
G06	VDD	POWER
G07	VDD	POWER
H03	VDD	POWER
H06	VDD	POWER
Ground		
A04	VSS	GROUND
A05	VSS	GROUND
A08	VSS	GROUND
B02	VSS	GROUND
B03	VSS	GROUND
B04	VSS	GROUND
B07	VSS	GROUND
C02	VSS	GROUND

Package Pad Location	Package Pad Name	Package Pad Function and Type
C03	VSS	GROUND
C05	VSS	GROUND
D01	VSS	GROUND
D06	VSS	GROUND
D07	VSS	GROUND
D08	VSS	GROUND
E04	VSS	GROUND
E07	VSS	GROUND
F01	VSS	GROUND
F05	VSS	GROUND
F07	VSS	GROUND
F08	VSS	GROUND
G04	VSS	GROUND
H02	VSS	GROUND
H05	VSS	GROUND
H07	VSS	GROUND
J01	VSS	GROUND
J04	VSS	GROUND
J05	VSS	GROUND
J08	VSS	GROUND

2.2 PINLIST – Package Configuration: TOP VIEW

Table 2.3. Pin List / Package Configuration – Top View

	8	7	6	5	4	3	2	1	
J	VSS	IN1	IP1	VSS	VSS	ON2	OP2	VSS	J
H	ON1	VSS	VDD	VSS	EN	VDD	VSS	IN2	H
G	OP1	VDD	VDD	VDD	VSS	VDD	VDD	IP2	G
F	VSS	VSS	VDD	VSS	VDD	VDD	EN*	VSS	F
E	VDD	VSS	VDD	VDD	VSS	VDD	SEL_7 MA	VDD	E
D	VSS	VSS	VSS	VDD	VDD	VDD	SLEEP*	VSS	D
C	ON4	VDD	FS_DIS ABLE	VSS	VDD	VSS	VSS	IN3	C
B	OP4	VSS	VDD	20KΩ TO VSS	VSS	VSS	VSS	IP3	B
A	VSS	IN4	IP4	VSS	VSS	OP3	ON3	N/C	A
	8	7	6	5	4	3	2	1	

3.0 Absolute Maximum Ratings (1)

Table 3.1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	MIN	MAX	Units
VDD	LVDS Power Supply		-0.3	3.6	V
VSS	LVDS Ground		-0.3	+0.3	V
$V_{IN, LVCMOS}$	LVCMOS Input / Output Signals		-0.3	VDD	V
IOS_sink (2)	Output Short Circuit Current	OP/ON = VDD, VDD = VDDMAX	4.0	8.0	mA
IOS_source (2)	Output Short Circuit Current	OP/ON = VSS, VDD = VDDMAX	-10.5	-5.9	mA
ESD_{HBM}	ESD Rating (HBM)		1000	-	V
ESD_{CDM}	ESD Rating (CDM)		500	-	V
Θ_{JC}	Thermal Resistance (junction to case)			12.7	°C/W
T_J	Junction Temperature			132	°C
T_{STG}	Storage Temperature		-65	125	°C
P_D (3)	Maximum package power dissipation			500	mW

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) TX drive current of 7mA selected, 50Ω load: Install 100Ω back-termination resistor (100Ω || 100Ω = 50Ω)
3) Per MIL-STD-883, method 1012.1, section 3.4.1, PD=(T_J (max) – T_C (max)) / Θ_{JC}

4.0 Operational Environment

Table 4.1: Operational Environment

Symbol	Parameter	Limit	Units
TID (1)	Total Ionizing Dose	1.0E5	rad(Si)
SEL (1)	Single Event Latch-up Immunity	≤100	MeV-cm^2/mg

5.0 Recommended Operating Conditions

Table 5.1: Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
VDD	LVDS Power Supply (2.5V ± 5%)	2.375	2.5	2.625	V
VSS	Ground		0		V
$V_{IN,LVDS}$	Input Voltage on any LVDS input pin	0.0		VDD	V
$V_{IN,LVCMOS}$	Input Voltage on any LVCMOS input pin	0.0		VDD	V
T_C	Case Temperature Range	-55		105	°C
T_j	Junction Temperature			125	°C

6.0 Electrical Characteristics

6.1 DC Electrical Characteristics

VDD=2.5V+/-5%, -55°C< T_C < +105°C, unless otherwise noted

Table 6.1.1: LVDS I/O DC Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
VCMR	Input Common Mode Voltage Range	VID = 150mV	0.1	1.25	VDD-0.1	V
VID_HYS	Differential Input Voltage Hysteresis	VCM = 1.25V		50		mV
ICS	Cold Spare Input Current IP/N	VIN = VDDMAX, VDD = VSS = 0V			150	µA
OCS	Cold Spare Output Current OP/N	VOUT = VDDMAX, VDD = VSS = 0V			50	µA
IIN_L	Input Current Low	IP, IN [1:4] = VSS	-150			µA
IIN_H	Input Current High	IP, IN [1:4] = VDD			150	µA
VOS (1, 2)	Output Common-Mode Offset Voltage	LVDS Outputs	1.25		1.40	V
ΔVOS (1, 2)	Change in VOS Between Complementary Logic States		-25		+25	mV
AIDD (2)	VDD Active Supply Current	K28.5 pattern @1.25Gbps			102	mA
QIDD (2)	VDD Quiescent Supply Current	EN/EN* Inactive (OP/ON Disabled)			75	mA
IDDSLP (2)	VDD Supply Sleep Current	SLEEP* Active			70	µA
V_{ID}	Input Amplitude, diff	Differential, Peak-to-Peak VCM = 1.25V	0.1		VDD	V
V_{OD} (1, 2)	Output Amplitude, diff.	Differential, Peak-to-Peak	250	330	400	mV
ΔV_{OD} (2)	Change in $V_{OD,LVDS}$ between complementary logic states	LVDS Outputs	-20		20	mV
P_{total} (2)	Power Dissipation	1.25Gbps, all channels operating		170	274	mW
CIN_P	Input Capacitance IP#	IP/IN to VSS			10	pF
CIN_N	Input Capacitance IN#				10	pF
COUT_P	Output Capacitance OP#	OP/ON to VSS			16	pF
COUT_N	Output Capacitance ON#				16	pF

Notes:

1) TX drive current of 3.5mA selected, 100Ω load: Do not install 100Ω back-termination resistor.
2) TX drive current of 7mA selected, 50Ω load: Install 100Ω back-termination resistor (100Ω || 100Ω = 50Ω)
3) Reference values only. Not guaranteed or tested

Table 6.1.2: LVCMOS I/O DC Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
VIH	CMOS high level input voltage		VDD*0.7	-	V
VIL	CMOS low level input voltage		-	VDD*0.3	V
IIH	CMOS high level input current	VIN=VDD	-	20	µA
IIL	CMOS low level input current	VIN=VSS	-10	-	µA
ICS	Cold-Spare Input Current	VIN = VDDMAX, VDD = VSS = 0V	-	10	µA

6.2 AC Electrical Characteristics

VDD=2.5V+/-5%, -55°C< TC < +105°C, unless otherwise noted.

Table 6.2.1: Timing Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
DR	Data Rate / Channel		0.002	1.25	Gbps
DC1 (3)	LVDS Output Duty Cycle	50% duty cycle input signal, 200MHz (1)	50.0	50.2	%
DC2 (3)	LVDS Output Duty Cycle	50% duty cycle input signal, 200MHz (2)	49.9	50.1	%
tPHLD1 (3)	LVDS High-Low Output prop. delay	100Ω load (1)	2.1	3.6	ns
tPLHD1 (3)	LVDS Low-High Output prop. delay		2.1	3.6	ns
tPHLD2 (3)	LVDS High-Low Output prop. delay	50Ω load (2)	2.0	3.5	ns
tPLHD2 (3)	LVDS Low-High Output prop. delay		2.0	3.5	ns
tHLT1 (3)	LVDS High-Low Output transition time	100Ω load (1)	665	676	ps
tLHT1 (3)	LVDS Low-High Output transition time		646	663	ps
tHLT2 (3)	LVDS High-Low Output transition time	50Ω load (2)	215	282	ps
tLHT2 (3)	LVDS Low-High Output transition time		215	277	ps
T_{J1} (3)	Total Jitter	CRPAT pattern		127	ps p-p
T_{J2} (3)	Total Jitter	625MHz clock pattern		5.0	ps rms
T_{EN} (3)	Device Output Enable time	Time from EN↑ & EN*↓ to ON/OP going active	3.3	5.6	ns
T_{DIS} (3)	Device Output Disable time	Time from EN↓ & EN*↑ to ON/OP going tri-state	1.5	3.1	ns
T_{SLEEP} (3)	Device sleep time	Time from SLEEP*↓ to ON/OP going tri-state (VOS)	3.3	5.8	ns
T_{WAKE} (3)	Device wake time	Time from SLEEP*↑ to ON/OP going active	2.4	3.4	us
$T_{FAILSAFE}$ (3)	Failsafe timeout after loss of signal	Time from VDIN<VTH, FS_DISABLE=VSS	0.3	1	us
T_{SKD1} (3)	Differential Output Pulse Skew	Channel-N |tPLHD-tPHLD|		30	ps
T_{SKCC} (3)	Output Channel to Channel Skew	All Channels |tPLHD-tPHLD|		50	ps

Notes:

1) TX drive current of 3.5mA selected, 100Ω load: Do not install 100Ω back-termination resistor.
2) TX drive current of 7mA selected, 50Ω load: Install 100Ω back-termination resistor (100Ω || 100Ω = 50Ω)
3) Guaranteed by Design

7.0 Packaging Drawings

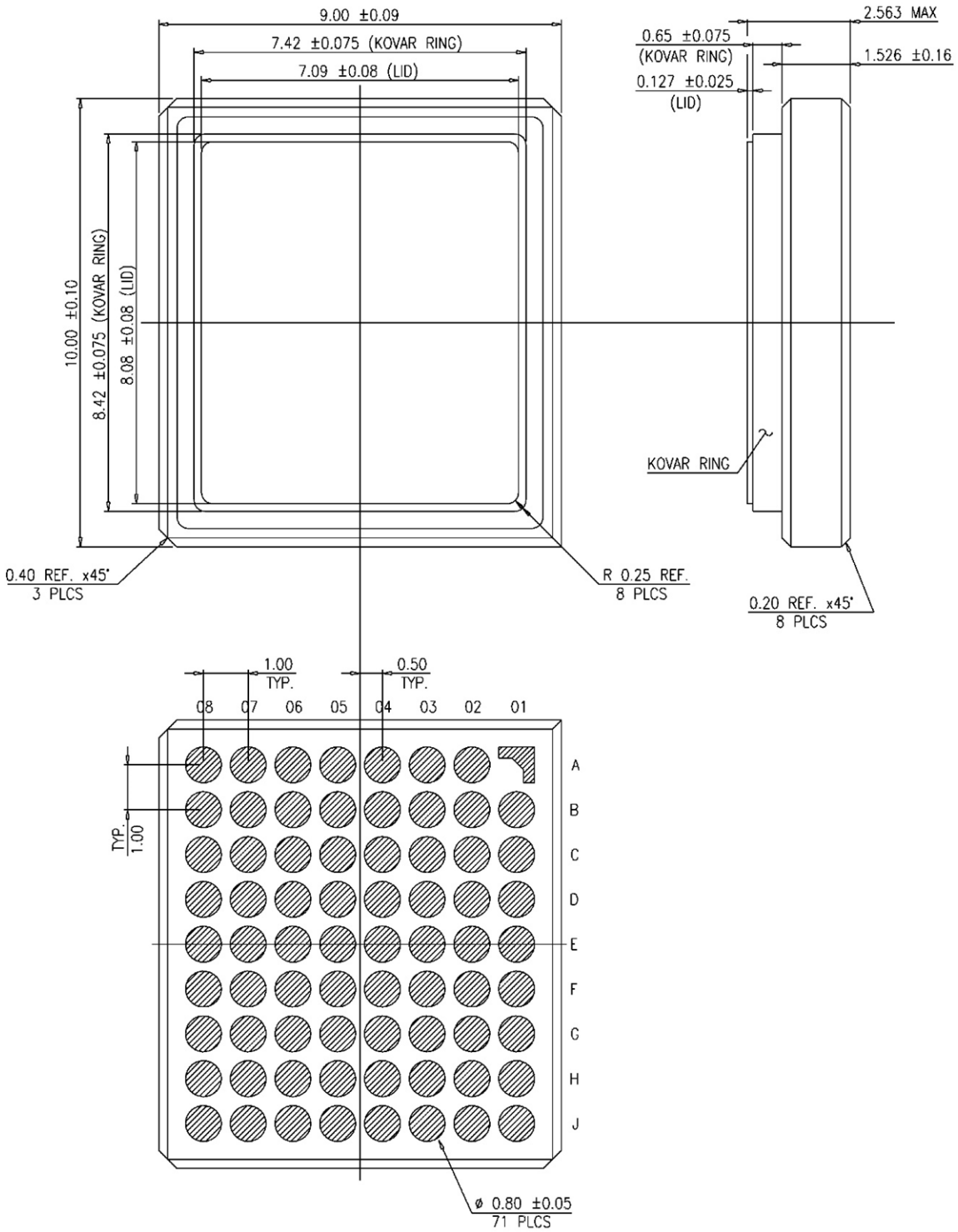

Figure 7.1: 71-Pin Ceramic Land Grid Array (C-LGA) Package

Notes:

1) Units are millimeters
2) LID is connected to VSS
3) Exposed-metal plating per MIL-PRF-38535 electroless nickel 4.0um nominal [2.54-8.89 limits] immersion gold 0.03-0.10um

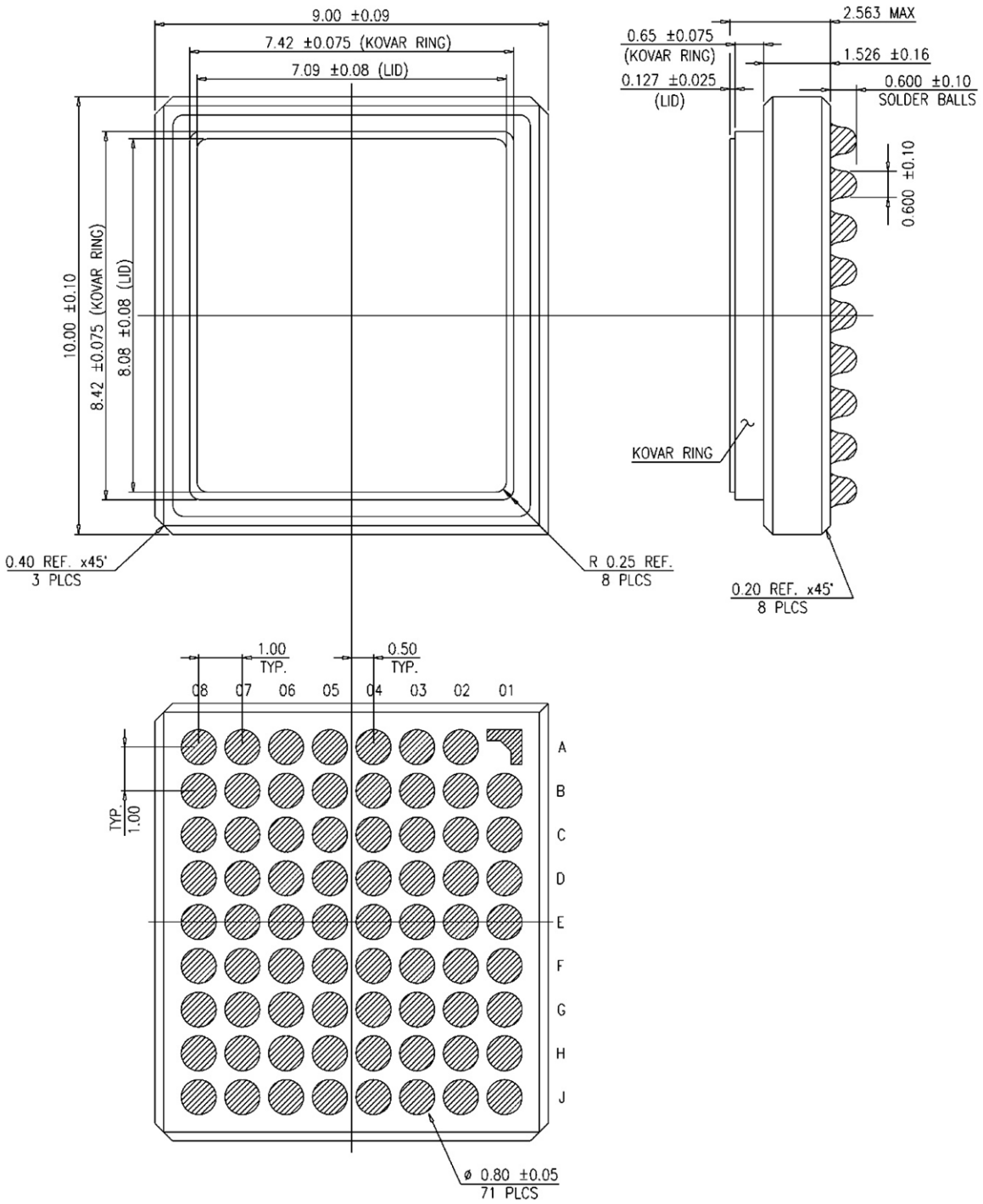

Figure 7.2: 71-Pin Ceramic Ball Grid Array (C-BGA) Package

Notes:

1) Units are Millimeters
2) LID is connected to VSS
3) Exposed-metal plating per MIL-PRF-38535 electroless nickel 4.0um nominal [2.54-8.89 limits] immersion gold 0.03-0.10um
4) Solder balls are 90Pb/10Sn composition, attached with 37Pb/63Sn Eutectic.
5) Solder balls are available for prototypes and engineering samples only, as they are not QML-qualified.
6) The dimensions shown for the attached solder balls are approximate.

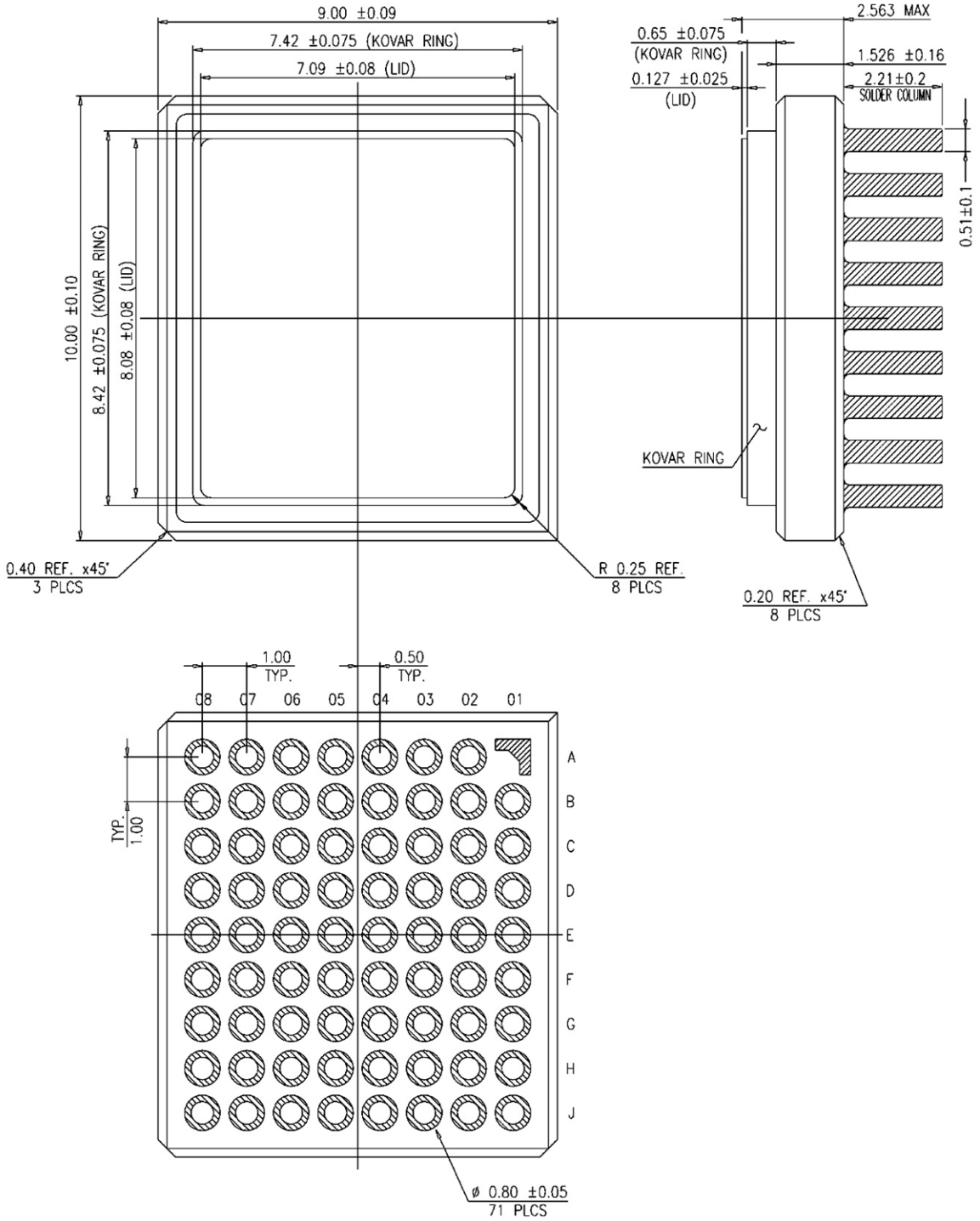

Figure 7.3: 71-Pin Ceramic Column Grid Array (C-CGA) Package

Notes:

1) Units are Millimeters
2) Lid is connected to VSS
3) Exposed-metal plating per MIL-PRF-38535 electroless nickel 4.0um nominal [2.54-8.89 limits] immersion gold 0.03-0.10um

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8.0 Ordering Information

8.1 CAES Part Number Ordering Information

Generic Datasheet Part Numbering

UTxxxxx * * * *

Lead Finish: (Notes: 1)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Screening Level: (Notes: 2, 3, 4, 5, 6, 7)
(P) = Prototype Flow (Temperature Range: 25°C only)
(F) = HiRel Flow (Temperature Range: -55°C to +105°C)

Case Outline: (Note: 6,7)
(Z) = 71-Ceramic Land Grid Array
(S) = 71-Ceramic Column Grid Array
(C) = 71-Ceramic Ball Grid Array

Radiation Hardness Assurance:
(-) = No RHA Assurance

UT54LVDS454 – High-Speed LVDS Repeater

Notes:

1) Lead finish (A, C, or F) must be specified.
2) Prototype Flow per CAES Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
3) HiRel Flow per CAES Manufacturing Flows Document. Radiation TID tolerance may not be ordered.
4) For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) packages, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column).
5) Contact factory to define alternative screening options
6) Ball Grid Array (BGA) Case Outline is only available for Prototype Flow Screening Level. (BGA Case Outline is not available for HiRel Flow Screening Level.)
7) All Case Outline options (i.e. LGA, BGA, CGA) are available for Prototype Flow Screening Level.

8.2 SMD Part Number Ordering Information

SMD Part Numbering

5962 * 21211 ** * * *

Lead Finish: (Notes: 1)
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Case Outline: (Note: 2)
(X) = 71-Ceramic Land Grid Array
(Y) = 71-Ceramic Column Grid Array

QML Class: (Note: 3)
(Q) = Class Q
(V) = Class V

Device Type:
(01) = UT54LVDS454 QML Q, V; (Temperature Range: -55C to +105C)
(02) = UT54LVDS454 QML Q+; (Temperature Range: -55C to +105C)

SMD Project Number:
(21211) = UT54LVDS454 High-Speed LVDS Repeater

Radiation Hardness Assurance: (Notes: 4)
(R) = 100 krad(Si)

Federal Stock Class Designator

Notes:

1) Lead finish (C or F) must be specified.
2) For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column).
3) Contact factory to determine alternative screening options.
4) A radiation hardness assurance level must be selected.

DATASHEET

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9.0 Revision History

Date	Revision	Change description
09/06/2018	0.0.1	Advanced Datasheet – Initial revision
10/23/2018	0.0.2	Advanced Datasheet – Update 1
10/30/2018	0.0.3	Advanced Datasheet – Update 2
02/05/2019	0.0.4	Advanced Datasheet – Update 3
08/28/2019	0.0.5	Preliminary Datasheet – Update 4
09/26/2019	0.0.6	Preliminary Datasheet – Update 5 – Incorporated Additional Review Comments
10/24/2019	0.0.7	Preliminary Datasheet – Update 6 – Updated Package Drawings: Figs. 7.1-3
10/28/2019	0.0.8	Preliminary Datasheet – Pin List/Config.: Table 2.2 Updated; Table 2.3 Added
01/28/2020	0.0.9	Preliminary Datasheet – Part No. Changed to UT54LVDS454
02/18/2020	0.1.0	Preliminary Datasheet – Updates to Section 6 Electrical Parameters
07/06/2020	0.2.0	Preliminary Datasheet – Updates to Table 6.1.1, p.9
07/21/2020	0.2.1	Section 8.1, p.14: Cobham P/N Ordering Info.: HiRel Flow: Letter "C" to "F"
09/14/2020	0.2.2	Updates to descriptions for both low/high data rate and cold spare operation
10/28/2020	1.2.3	Section 6.1, Table 6.1.1, p.10: ICS, OCS, IIN_L, IIN_H
03/31/2021	1.3.0	Updated Product Description: a) Dual, Full-Duplex, or b) Quad, Simplex Repeater; Added SMD Number, p.1,17; Added Table 1.1, p.5: Logic Function Truth Table; Updated Table 6.1.1, p.10: CIN_P,N, COUT_P,N Updates; Updated Table 6.2.1, p.11: Electrical Parameter Updates; Updated Section 8.0, p.16,17: Ordering Information
06/24/2021	1.3.1	Added QML Q+ ordering option, Device Type 02, to Section 8.2, p.16: SMD Part Number Ordering Information
08/04/2021	1.3.2	Corrected VOS range, p.4, UT54LVDS454 Output Driver description
08/24/2021	1.3.3	AMR Table, p.9: Updated HBM ESD rating to reflect lowest pin voltage
09/10/2021	1.3.4	Correction:"High-Speed" throughout, Table 4.1, p.9: Removed Note 1.
12/03/2021	1.3.5	Move IOS_source/sink specs. from p.10, Table 6.1.1 to p.9, Table 3.1. Changed from "Preliminary" to "Released." Features, p.1: Changed QML status to QML-V pending
12/15/2021	1.3.6	Corrections to Sections 8.1, 8.1, Part Number Ordering Info., p.15,16
01/13/2022	1.3.7	AMR Table, p.9: Added CDM ESD rating.

DATASHEET

RELEASED 01/13/22

1.25 Gbps LVDS Repeater

UT54LVDS454

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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