DATASHEET

RELEASED 03/23/22

3.125 Gbps Crosspoint Switch (XPS)

UT65CML8X8FD

Features

- 8 x 8, Full Duplex Crosspoint Switch Matrix
- Data Rates up to 3.125 Gbps per Channel
- Protocol Independent
- Low Latency
- Low Channel-to-Channel Skew
- SPI Port Control Interface
- Diagnostic Serial Loopback Mode
- Low Power Dissipation
- Separate Power Domains per Bank
- Power Down Feature for Unused Lanes
- Loss of Signal (LOS) Detect
- Adjustable 50 Ω High-Speed Terminations
- Standard Microelectronics Drawing (SMD):
  - 5962-17213 (QML-Q, V Pending)
- Package Information:
  - 143-Pin Ceramic Land Grid Array (C-LGA)
    - Base Package (Pads Only)
  - Ceramic Column Grid Array (C-CGA)
    - Flight Units
  - Ceramic Ball Grid Array (C-BGA)
    - Prototypes
  - Small Size: 14.5 x 14.5 mm; 1 mm Pad Pitch

Operational Environment

- Temperature Range: -55°C ≤ Tc ≤ +105°C
- Total Dose: $1x10^5$ rad(Si)
- SEL Immune: ≤ 100 MeV·cm^2/mg
- SET-BER: $7x10^{-17}$ errors/dev-day

Applications

- High Speed Serial Repeater and Distribution Applications
- Primary and Redundant Data Switching
- Port Replication
- Space VPX (VITA78) Data Plane Switches
- High Speed 2:1 MUX + 1:2 DEMUX Functions

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Introduction

The emerging VITA78, Space VPX, standard specifies a data plane switch function which enables a redundant and cross strapped serial data path within the VPX chassis. Typically, a primary serial I/O based resource is cross strapped with a redundant resource. There can also be redundant resources configured in a non-cross strapped configuration. This 8 x 8 cross point device can support implementation of either scenario.

Because the switch is purely a cross bar, it is protocol-independent. This makes the switch very versatile and can be applied in proprietary architectures, in addition to the Serial Rapid IO protocol specified in VITA78. The loop back feature, available at each four lane XAUI interface, is very useful for system diagnostics, test, and optimization.

Two key advantages of the device are its small size and low power. Any unused lanes can be powered down, and if the device is placed in close proximity to the source device (e.g. the serial data path is less than 1 or 2 cm), the TX driver can be run in half power mode.

The primary function of the Space VPX 8 x 8 Crosspoint Switch is to perform switching of 10G XAUI serial data streams between one of two, full duplex, current-mode logic (CML) signal I/O pads. The primary I/O configuration is an 8 x 8 XAUI-compatible port switch matrix; each port has four full duplex lanes operating at up to 3.125 Gbps.

Inputs include Receiver (RX) Equalization (EQ) to compensate for input losses. The input signal is then routed through a MUX to the selected output channel. Output Transmit (TX) De-Emphasis (DE) is not currently supported. The Cross Point Switch does not include input Clock and Data Recovery (CDR), and so operates as a Repeater and not a Re-timer.

The MUX switches which determine the core matrix configuration are set via the 4-wire SPI register port.

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1.0 Functional Description

1.1 Overview

Figure 1 illustrates the functionality of the Crosspoint Switch (XPS). The device is comprised of 4 banks, each containing 4 individual lanes. Each lane can be individually enabled for transmit only, receive only, or full-duplex operation.

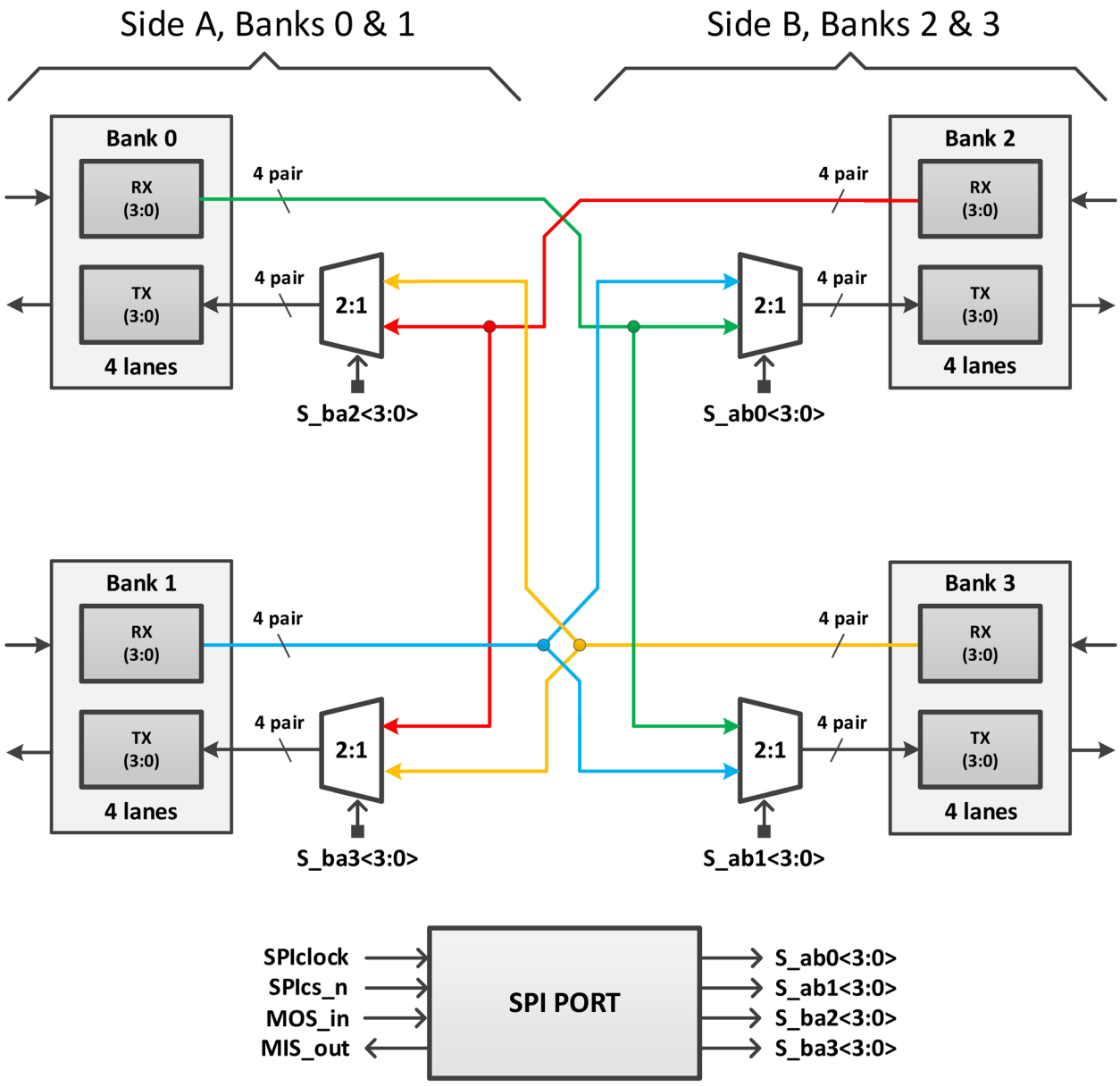

Figure 1: Block Diagram

The Crosspoint Switch functionality is illustrated in figures 2 and 3. Individual lanes or groups of lanes within a bank can be routed directly, as an A-B Crosspoint, or broadcasted to associated banks.

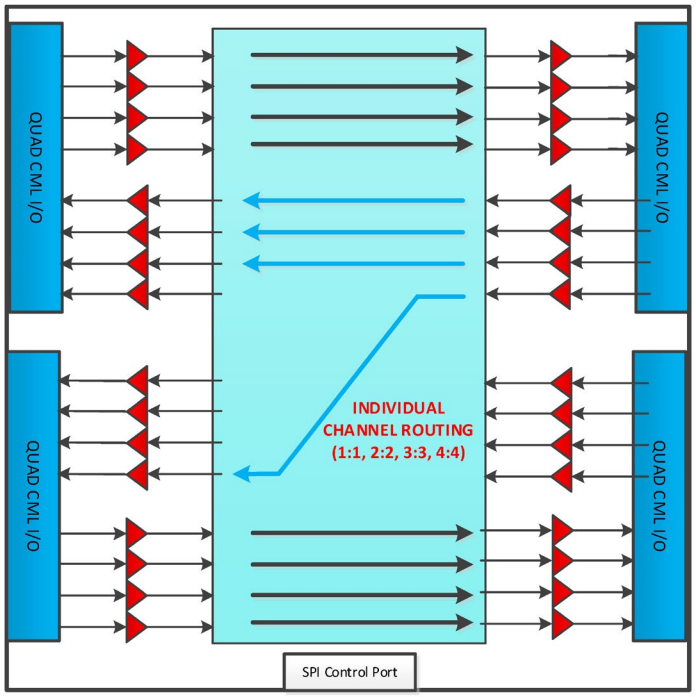

Figure 2: Crosspoint Switch Individual Channel Routing

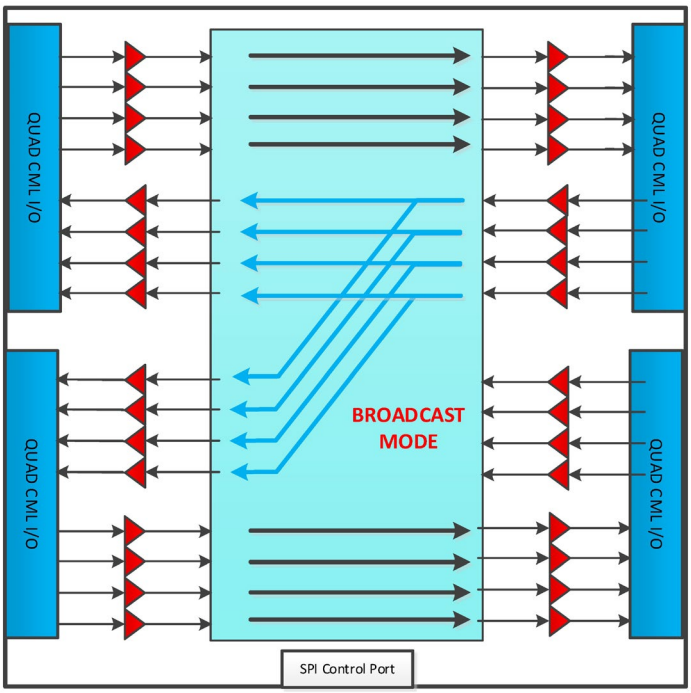

Figure 3: Broadcasting One Input Bank to Two Output Banks

The serial loop-back function is illustrated in Figure 4. Serial data present at the receiver inputs is looped back and re-transmitted within the same lane in the same bank. This function is provided to the system developer for de-bugging and continuity check purposes.

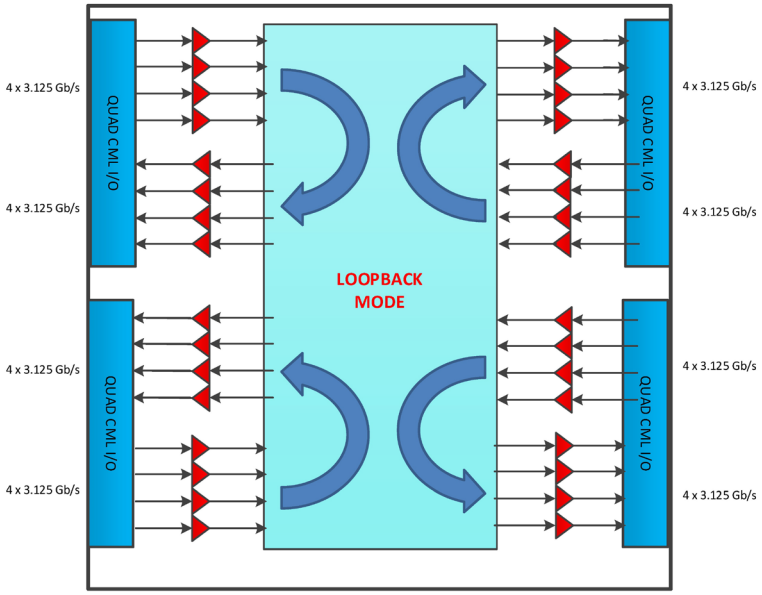

Figure 4: Serial RX to TX Loopback Mode for System De-Bugging

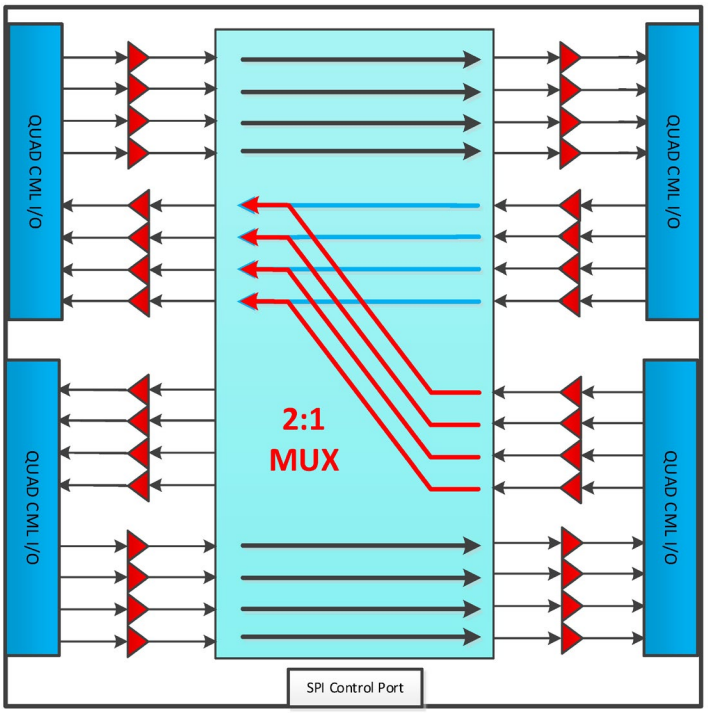

Figure 5: Crosspoint 2:1 MUX Function

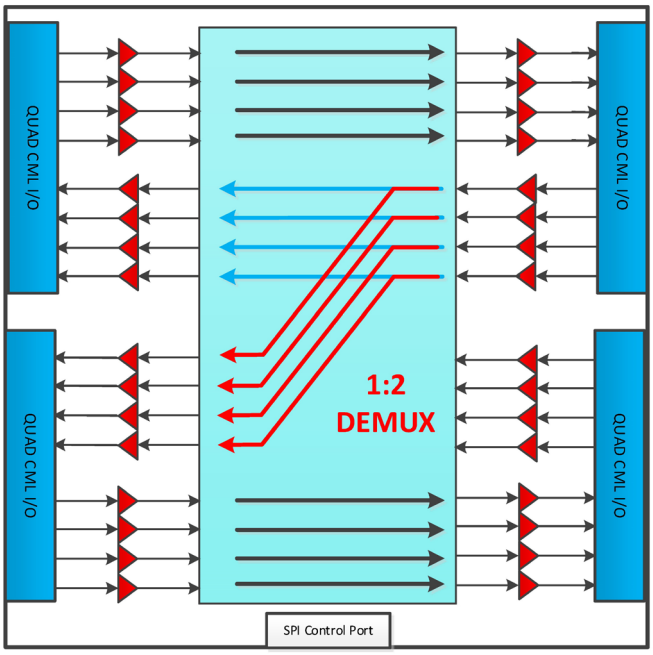

Figure 6: Crosspoint 1:2 DEMUX Function

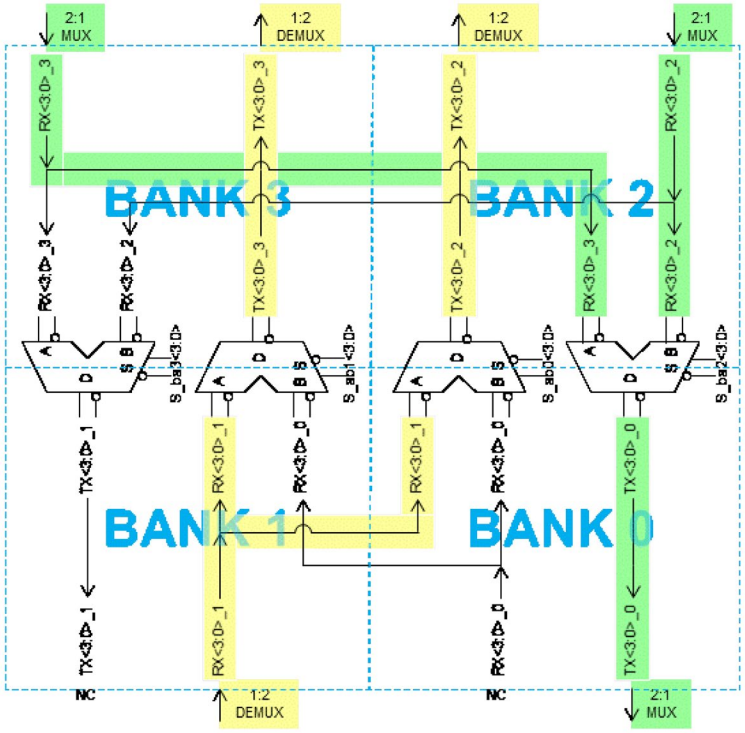

Figure 7: Implementation of Single XPS 2:1 MUX (Green) and 1:2 DEMUX (Yellow) Functions

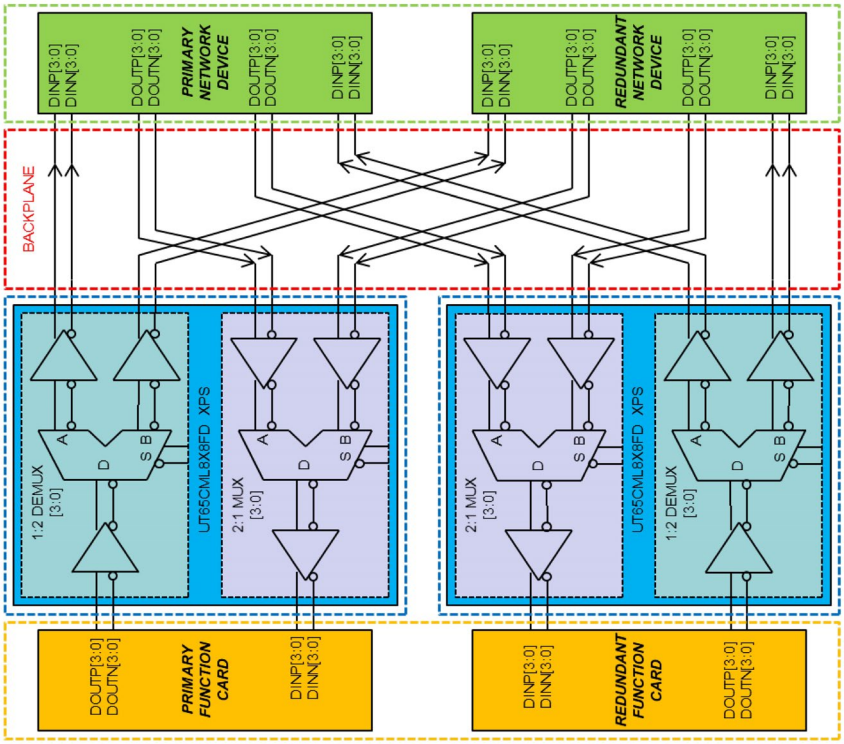

Figure 8: Crosspoint Full Redundancy A-B Cross-Strapping Using Two XPS Devices

1.2 Input Receiver (RX)

The Receiver (RX) input buffers operate using the current-mode logic (CML) I/O standard and are terminated into 50Ω. The input buffers accept an input amplitude range of 100-800 mV p-p single-ended, or 200-1600 mV p-p differential. The input termination is tunable over a narrow resistor value range in order to provide adjustment for process variation to approximately 50Ω input impedance for best signal integrity (SI). An input receiver equalizer is provided to compensate for channel losses. The Rx EQ is composed of a Continuous Time Linear Equalizer (CTLE) circuit with programmable settings. Each receiver equalizer circuit can be programmed to one of 32 values. These values are set through internal registers EQ_0-3_0-3<0:4> via the SPI Port interface. An input Loss of Signal (LOS) detect function is supported for system-level monitoring and fault handling. When enabled, if the input signal edge rate falls below 10 MHz, the LOS detect function squelches all associated transmitter outputs. The LOS function is enabled via internal registers EN_LOS_0-3<0:3>. The status of the LOS function for any port can be observed by reading SPI registers HEX 27 or 28 <7:0>.

1.3 Output Transmitter (TX)

The Transmitter (TX) output drivers operate using the current mode logic (CML) I/O levels. Each output is terminated into 50 or 100 Ω differentially. No output Pre-Emphasis is provided as the device is not a data re-timer. The output termination is selectable over a narrow resistor value range in order to provide adjustment for process variation. The output TX amplitude is programmable using internal registers TX_I_0-1<0:31>, which set the output drive currents. The output amplitude range is 200-600 mV p-p single-ended, or 400-1200 mV p-p differential. Selecting a drive current sufficient to achieve error-free communications, yet less than the maximum available minimizes power consumption.

Note: Both RX inputs and TX outputs must be AC-coupled using broadband 0.1μF (100nF) capacitors. The intended XPS application is for the XAUI specification using 8b/10b encoding as part of RapidIO and SpaceVPX requirements, as well as other DC balanced data formats.

1.4 Serial Peripheral Interface (SPI) PORT

1.4.1 Overview

The Serial Peripheral Interface (SPI) bus is a simple, synchronous, full duplex, 4-wire serial communications interface in a Master-Slave device configuration. SPI supports single, or multiple slave devices. There is always only one master device. Although there is no formal SPI bus standard, it is widely used, with many variations in existence. Data is clocked out of the Master device on the MOSI pin to a selected Slave device. One bit is transmitted or received on every SPIclock edge or one byte for eight clock cycles. The SPIcs_n signal is de-asserted to indicate boundaries between command and data words, or to terminate communication between devices. Because SPI is a primitive protocol, there is no acknowledgement bit (ACK) available. Correct data transmission is verified by reading the selected register byte in question.

1.4.2 SPI Advantages

- Full duplex communication
- Faster data transfer than the I2C or SM bus standards
- Simple hardware interfacing
- Slave devices don't require a unique address
- A simple protocol for connecting Master and Slave devices
- Tolerant of clock period variation
- Serial or parallel configurations allow multiple devices to share the same Master SPI port

1.4.3 Signals

Table 1 lists the Serial Peripheral Interface signals and their directions and functions.

Table 1: SPI Bus Signals

Signal Name	Signal Description	Signal Direction
SPIclock	SPI Serial Clock	From Master to Slave device
MOS_in	Master Out / Slave In	From Master to Slave device
MIS_out	Master In / Slave Out	From Slave to Master device
SPIcs_n	Slave Chip Select, Active Low	From Master to Slave device

1.4.4 SPI Bus Configurations

Figure 9a shows a simple point to point SPI configuration. Command and data word operations are conducted in single byte transactions separated by SPIcs_n assertions.

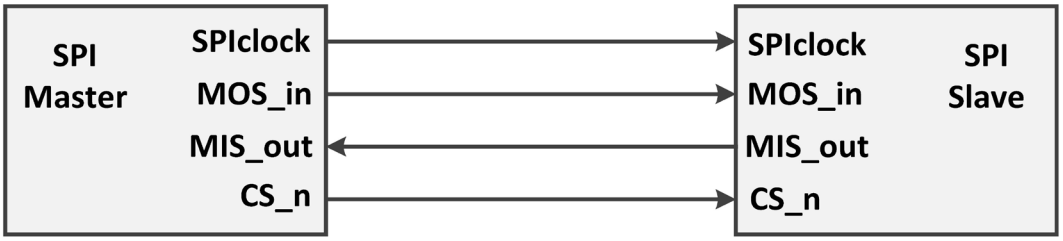

Figure 9a: Master, single slave – Point-to-point configuration

Figure 9b illustrates multiple parallel Slave devices controlled by a single Master device. While command and data word operations are conducted in single byte transactions, each Slave device has a unique SPIcs_n selection signal.

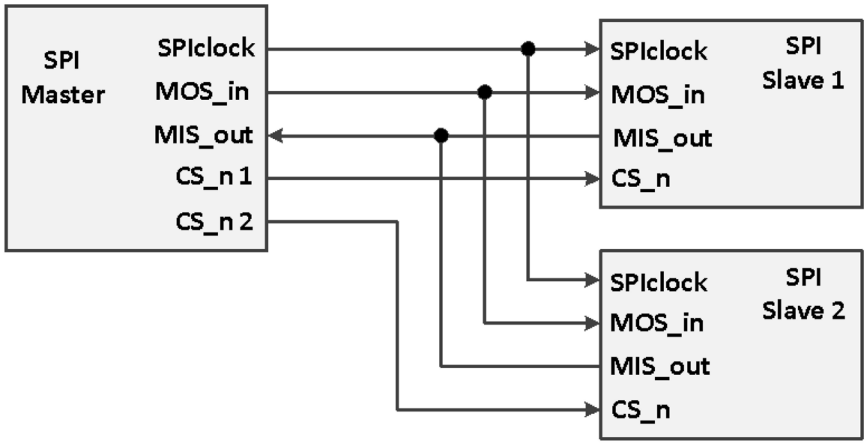

Figure 9b. Single master, multiple slaves - Parallel configuration

Figures 9c, 9d illustrate multiple serially-connected (i.e. daisy chain) slave devices controlled by a single master device. Command and data word operations are conducted as a string of serially transmitted, byte-wide transactions. For N devices connected in serial, N bytes are transmitted back to back. The SPIcs_n signal remains enabled for the duration of multiple command or data word operation. For the example of Figure 9thec, 2 bytes of command or data information are transmitted with SPIcs_n active for 16 clock cycles, when x2 SPI Port devices are daisy-chained, as depicted in Figure 9c. As a result, the Slave device FIFOs receive the byte intended for them. Information for the most distant device is transmitted first, and the closest last. Figure 9d shows an example timing diagram for the daisy chain circuit of Figure 9c.

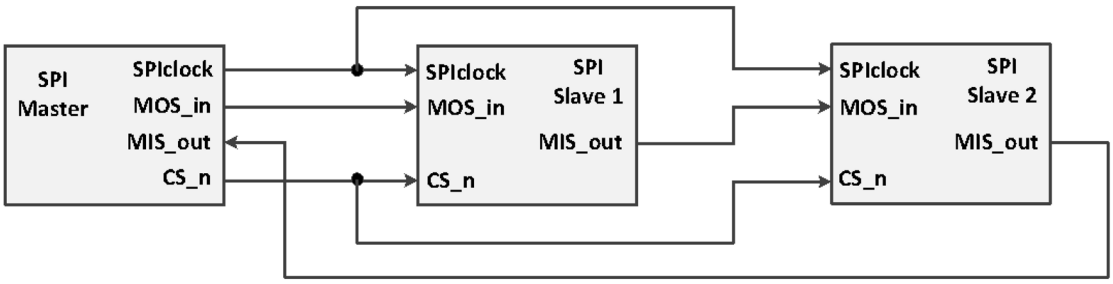

Figure 9c: Single master, multiple slaves - Daisy Chain configuration: Block Diagram

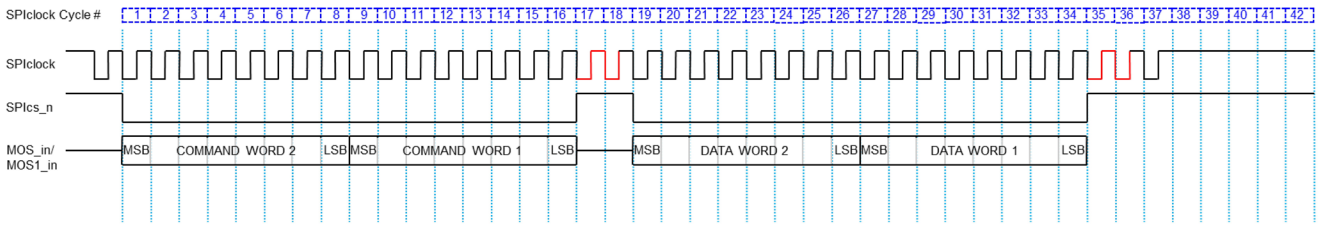

Figure 9d: Single master, multiple slaves - Daisy Chain configuration: Timing Diagram

Notes:

1) Command & Data Word 1 correspond to SPI Slave 1 device
2) Command & Data Word 2 correspond to SPI Slave 2 device
3) MOS_in & MIS_out correspond to SPI Master device
4) MOS1_in corresponds to SPI Slave 1 device

1.4.5 SPI Interface Reset

Figure 10 illustrates the SPI port reset and general timing. When the Crosspoint switch is powered, its internal power-on reset (POR) places the SPI port in a reset condition. The user must supply at least 6 clocks to bring the part out of reset. The chip select signal (SPIcs_n, active low) is asserted at the falling edge of SPIclock ①. In a SPI transaction, a command word is issued first. Its 7 most significant bits address the control register in question, while the least significant bit indicates whether a read or write operation is requested. A data word follows the command word to be written, or the results of a read, and will be shown in detail in the following sections. Upon completion of a command or data transaction, a minimum of two SPIclock cycles are required to register the transaction. The order and number of READs and WRITEs is not critical to SPI port operation. SPIclock can and should be stopped after communication is complete.

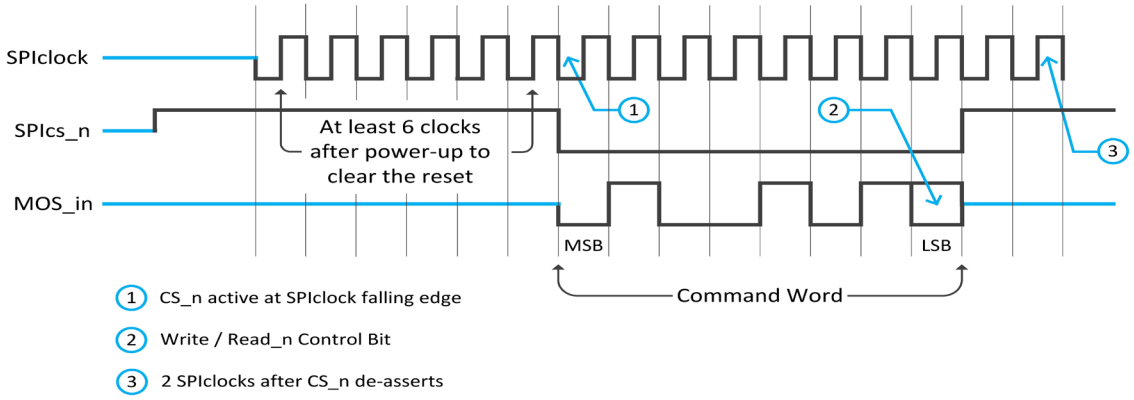

Figure 10: SPI Reset and General Timing

1.4.6 SPI WRITE

A SPI WRITE operation is shown in Figure 11. The command word LSB indicates a WRITE operation to address Hex 15. The command word LSB on MOS_in ("MOSI"), when set to a 1, indicates a WRITE operation. The data word indicates the data to be written to that location. The chip select SPIcs_n is enabled on the falling edge of SPIclock. After a SPI interface reset, only one clock is required to begin a SPI transaction. Following a command or data word, a minimum of 2 SPIclock cycles are required to register the transaction.

If the previous 8-bit sequence is a WRITE command or WRITE data, then the current 8-bit sequence on MIS_out ("MISO") is undefined/don't care.

A "continuous" or sequential WRITE operation is supported by the XPS SPI Port. MIS_out ("MISO") can repeatedly write to selected addresses, i.e. WRITE command word+ data pairs on MOS_in ("MOSI"), continuously, until all WRITEs are completed (e.g. all XPS registers are written).

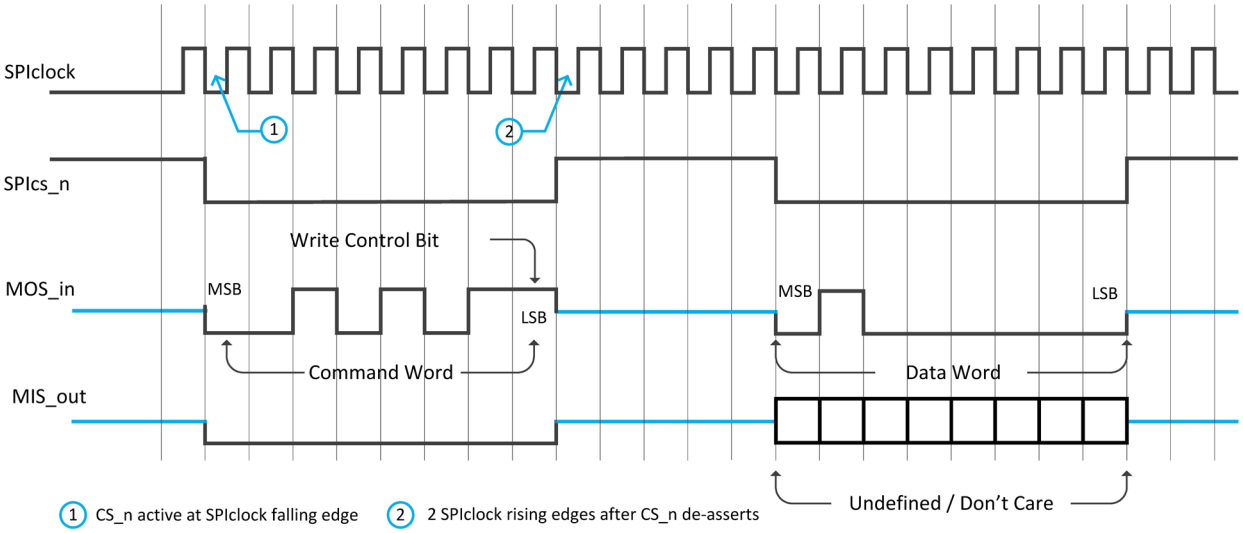

Figure 11: SPI Port WRITE operation

1.4.7 SPI READ

A SPI READ operation is shown in Figure 12. The command word LSB indicates a READ operation from address Hex 15. The command word LSB on MOS_in ("MOSI"), when set to a 0, indicates a READ operation. The data word indicates the data to be read from that location. Following a data or command word, a minimum of 2 SPIclock cycles are required to register the transaction. Data transmitted on MIS_out ("MISO") corresponds to the addressed register value of the previous READ command. The MIS_out ("MISO") data is transmitted on the negative edge of SPIclock. The first bit is valid data as SPIcs_n is asserted and active at the negative-edge of the SPIclock.

If the previous 8-bit sequence is a READ-command, then the data output on MIS_out ("MISO"), i.e. the current 8-bit sequence, is valid and corresponds to that READ-command.

A "continuous" or sequential READ operation is supported by the XPS SPI Port. MIS_out ("MISO") can repeatedly output addressed data as selected by address, i.e. READ Command Word on MOS_in ("MOSI"), until all READs are completed (e.g. all XPS registers are read).

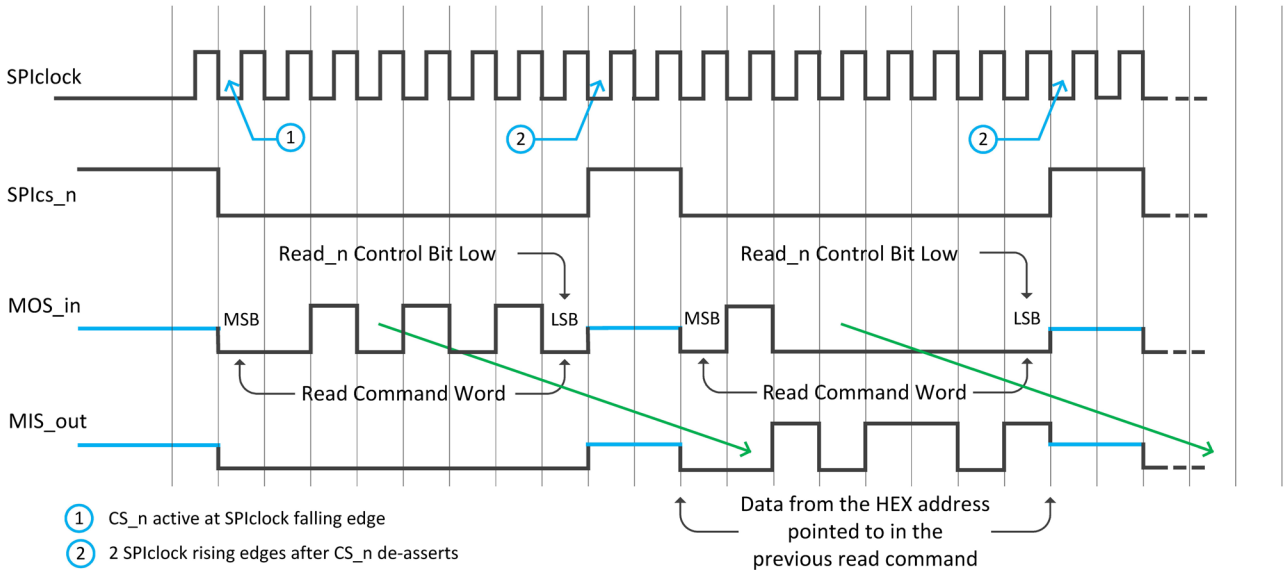

Figure 12: SPI Port Read operation

1.4.8 SPI Port Safety Feature

If the number of bits shifted out on the MOS_in ("MOSI") is not a multiple of 8, the command will be ignored or dropped. If a WRITE command is a multiple of 8 bits, but the following data word was not, the WRITE command and the data word will be dropped. In either of these two cases, the WRITE command will need to be re-transmitted.

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2.0 Pinlist

2.1 Pinlist – Table Format

Table 2: Pin List – Pin I/O Function Type Key – Table Format

Abbreviation	Description
CML-O	CML Compatible Output
CML-I	CML Compatible Input
SPI-I	LVCMOS Compatible Input-SPI Port Only
SPI-O	LVCMOS Compatible Output-SPI Port Only
COB	CAES Use Only
VDD	Power Supply
VSS	Ground

Table 2: Pin List – Pin Description – Table Format (Continued)

Number	Name	Type	Description
CML Transmitters (TX)			
A3	TXP_0_0	CML-O	CML Output, Positive
A4	TXN_0_0	CML-O	CML Output, Negative
B1	TXP_1_0	CML-O	CML Output, Positive
B2	TXN_1_0	CML-O	CML Output, Negative
D1	TXP_2_0	CML-O	CML Output, Positive
D2	TXN_2_0	CML-O	CML Output, Negative
F1	TXP_3_0	CML-O	CML Output, Positive
F2	TXN_3_0	CML-O	CML Output, Negative
E12	TXP_0_1	CML-O	CML Output, Positive
E11	TXN_0_1	CML-O	CML Output, Negative
C12	TXP_1_1	CML-O	CML Output, Positive
C11	TXN_1_1	CML-O	CML Output, Negative
A12	TXP_2_1	CML-O	CML Output, Positive
A11	TXN_2_1	CML-O	CML Output, Negative
A8	TXP_3_1	CML-O	CML Output, Positive
A7	TXN_3_1	CML-O	CML Output, Negative
H1	TXP_0_2	CML-O	CML Output, Positive
H2	TXN_0_2	CML-O	CML Output, Negative
K1	TXP_1_2	CML-O	CML Output, Positive
K2	TXN_1_2	CML-O	CML Output, Negative
M1	TXP_2_2	CML-O	CML Output, Positive
M2	TXN_2_2	CML-O	CML Output, Negative
M5	TXP_3_2	CML-O	CML Output, Positive
M6	TXN_3_2	CML-O	CML Output, Negative
M10	TXP_0_3	CML-O	CML Output, Positive
M9	TXN_0_3	CML-O	CML Output, Negative
L12	TXP_1_3	CML-O	CML Output, Positive
L11	TXN_1_3	CML-O	CML Output, Negative
J12	TXP_2_3	CML-O	CML Output, Positive
J11	TXN_2_3	CML-O	CML Output, Negative
G11	TXP_3_3	CML-O	CML Output, Positive
G12	TXN_3_3	CML-O	CML Output, Negative

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CML Receivers (RX)			
B6	RXP_0_0	CML-I	CML Input, Positive
B5	RXN_0_0	CML-I	CML Input, Negative
C3	RXP_1_0	CML-I	CML Input, Positive
C4	RXN_1_0	CML-I	CML Input, Negative
D5	RXP_2_0	CML-I	CML Input, Positive
D6	RXN_2_0	CML-I	CML Input, Negative
E3	RXP_3_0	CML-I	CML Input, Positive
E4	RXN_3_0	CML-I	CML Input, Negative
F10	RXP_0_1	CML-I	CML Input, Positive
F9	RXN_0_1	CML-I	CML Input, Negative
D10	RXP_1_1	CML-I	CML Input, Positive
D9	RXN_1_1	CML-I	CML Input, Negative
B10	RXP_2_1	CML-I	CML Input, Positive
B9	RXN_2_1	CML-I	CML Input, Negative
C8	RXP_3_1	CML-I	CML Input, Positive
C7	RXN_3_1	CML-I	CML Input, Negative
G3	RXP_0_2	CML-I	CML Input, Positive
G4	RXN_0_2	CML-I	CML Input, Negative
J3	RXP_1_2	CML-I	CML Input, Positive
J4	RXN_1_2	CML-I	CML Input, Negative
L3	RXP_2_2	CML-I	CML Input, Positive
L4	RXN_2_2	CML-I	CML Input, Negative
K5	RXP_3_2	CML-I	CML Input, Positive
K6	RXN_3_2	CML-I	CML Input, Negative
L8	RXP_0_3	CML-I	CML Input, Positive
L7	RXN_0_3	CML-I	CML Input, Negative
K10	RXP_1_3	CML-I	CML Input, Positive
K9	RXN_1_3	CML-I	CML Input, Negative
J8	RXP_2_3	CML-I	CML Input, Positive
J7	RXN_2_3	CML-I	CML Input, Negative
H10	RXP_3_3	CML-I	CML Input, Positive
H9	RXN_3_3	CML-I	CML Input, Negative

SPI Port			
F7	MOS_in	SPI-I	Master Out Slave In (“MOSI”)
G7	MIS_out	SPI-O	Master In Slave Out (“MISO”)
F8	SPIclock	SPI-I	SPI Clock (“SCK”)
G8	SPIcs_n	SPI-I	Chip Select Bar (“/CS”, “/SS”)

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CAES-Only Functions			
D3	-	COB	CAES Use Only – 10KΩ to VSS
D8	-	COB	CAES Use Only - 10KΩ to VSS
E8	-	COB	CAES Use Only - 10KΩ to VDD_25
F4	-	COB	CAES Use Only - 10KΩ to VSS
F5	-	COB	CAES Use Only - No Connect (N/C)
F6	-	COB	CAES Use Only - 10KΩ to VSS
G5	-	COB	CAES Use Only - 10KΩ to VSS
G6	-	COB	CAES Use Only - 10KΩ to VSS
H7	-	COB	CAES Use Only - 10KΩ to VDD_25

Power			
C6, C10, E7, E10, H5, J10, K3, K7	VDD	VDD	Core Power
H6, E6	VDDA_BIAS_[1:0]	VDD	Analog Bias Power 1,0
K12, J1, D12, C1	VDDARX_[3:0] (1)	VDD	Analog CML Receive (RX) Power
M11, L1, B12, A2	VDDATX_[3:0] (1)	VDD	Analog CML Transmit (TX) Power
H12, G1, F12, E1	VDDRX_[3:0] (1)	VDD	CML Receive (RX) Power
M7, M3, A9, A6	VDDTX_[3:0] (1)	VDD	CML Transmit (TX) Power
G10	VDD_25	VDD	CMOS Power-SPI Port

Ground			
A5, A10, B3, B4, B7, B8, B11, C2, C5, C9, D4, D7, D11, E2, E5, E9, F3, F11, G2, G9, H3, H4, H8, H11, J2, J5, J6, J9, K4, K8, K11, L2, L5, L6, L9, L10, M4, M8, M12	VSS	VSS	Transmit, Receive, Core Ground

Note:

1) There are separate VDDARX, VDDATX, VDDRX, VDDTX pins for each bank. This is indicated by the bus notation suffix: _[3:0]. All four pins for each bank supply are connected to their respective common power supply.

2.2 Pinlist – Package Configuration: Top View

Table 3. Pin List / Package Configuration

	12	11	10	9	8	7	6	5	4	3	2	1	
M	VSS	VDDA TX_3	TXP _0_3	TXN _0_3	VSS	VDD TX_3	TXN _3_2	TXP _3_2	VSS	VDD TX_2	TXN _2_2	TXP _2_2	M
L	TXP _1_3	TXN _1_3	VSS	VSS	RXP _0_3	RXN _0_3	VSS	VSS	RXN _2_2	RXP _2_2	VSS	VDDA TX_2	L
K	VDDA RX_3	VSS	RXP _1_3	RXN _1_3	VSS	VDD	RXN _3_2	RXP _3_2	VSS	VDD	TXN _1_2	TXP _1_2	K
J	TXP _2_3	TXN _2_3	VDD	VSS	RXP _2_3	RXN _2_3	VSS	VSS	RXN _1_2	RXP _1_2	VSS	VDDA RX_2	J
H	VDD RX_3	VSS	RXP _3_3	RXN _3_3	VSS	VDD _25	VDDA _BIAS _1	VDD	VSS	VSS	TXN _0_2	TXP _0_2	H
G	TXN _3_3	TXP _3_3	VDD _25	VSS	SPI cs_n	MIS _out	VSS	VSS	RXN _0_2	RXP _0_2	VSS	VDD RX_2	G
F	VDD RX_1	VSS	RXP _0_1	RXN _0_1	SPI clock	MOS _in	VSS	N/C	VSS	VSS	TXN _3_0	TXP _3_0	F
E	TXP _0_1	TXN _0_1	VDD	VSS	VDD _25	VDD	VDDA _BIAS _0	VSS	RXN _3_0	RXP _3_0	VSS	VDD RX_0	E
D	VDDA RX_1	VSS	RXP _1_1	RXN _1_1	VSS	VSS	RXN _2_0	RXP _2_0	VSS	VSS	TXN _2_0	TXP _2_0	D
C	TXP _1_1	TXN _1_1	VDD	VSS	RXP _3_1	RXN _3_1	VDD	VSS	RXN _1_0	RXP _1_0	VSS	VDDA RX_0	C
B	VDDA TX_1	VSS	RXP _2_1	RXN _2_1	VSS	VSS	RXP _0_0	RXN _0_0	VSS	VSS	TXN _1_0	TXP _1_0	B
A	TXP _2_1	TXN _2_1	VSS	VDD TX_1	TXP _3_1	TXN _3_1	VDD TX_0	VSS	TXN _0_0	TXP _0_0	VDDA TX_0		A
	12	11	10	9	8	7	6	5	4	3	2	1	

3.0 Absolute Maximum Ratings (1)

Table 4: Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
VDD	Core Supply Voltage	-0.5	1.76	V
VSS	Ground Voltage	-0.5	+0.5	V
VDDA_BIAS_[1:0]	Analog Bias Supply Voltage	-0.5	1.76	V
VDDARX_[3:0] (2)	Analog CML Receiver (RX) Supply Voltage	-0.5	1.76	V
VDDATX_[3:0] (2)	Analog CML Transmitter (TX) Supply Voltage	-0.5	1.76	V
VDDRX_[3:0] (2)	CML Receiver (RX) Supply Voltage	-0.5	1.76	V
VDDTX_[3:0] (2)	CML Transmitter (TX) Supply Voltage	-0.5	2.65	V
VDD_25	SPI Port Supply Voltage	-0.5	3.85	V
IOS_LVCMOS	LVCMOS Output Short Circuit Current	-200	200	mA
VIO_LVCMOS	LVCMOS Input / Output Signal Voltage	-0.5	3.85	V
IINDC_CML	DC Input Current, CML Inputs	-10	10	mA
IINDC_LVCMOS	DC Input Current, LVCMOS Inputs	-10	10	mA
ESD_CML	CML ESD Rating (HBM)	1 k	-	V
ESD_NON-CML	Non-CML ESD Rating (HBM)	2 k	-	V
P_D (3)	Maximum Power Dissipation		2.5	W
Θ_{JC}	Thermal Resistance (junction to case)		10.0	°C/W
T_J	Junction Temperature		130	°C
T_{STG}	Storage Temperature	-65	125	°C

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) There are separate VDDARX, VDDATX, VDDRX, VDDTX pins for each bank. This is indicated by the bus notation suffix: _[3:0]. All four pins for each bank supply are connected to their respective common power supply.
3) Per MIL-STD-883, method 1012.1, section 3.4.1, $P_{D(PACKAGE)}=(T_{J(max)} - T_{C(max)}) / \Theta_{JC}$

4.0 Operational Environment

Table 5: Operational Environment

Symbol	Parameter	Limit	Units
TID (1)	Total Ionizing Dose	$1x10^5$	rad(Si)
SEL	Single Event Latch-up	100	MeV·cm²/mg
SEU/SEFI	Single Event Upset (Onset LET)	77.7	MeV·cm²/mg
SET-BER (2)	Single Event Transient induced Bit Error Rate	$7x10^{-17}$	errors/dev-day

Notes:

1) Irradiated at dose rate = 50 - 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A
2) Adams 90% Geosynchronous orbit

5.0 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Parameter	Conditions	MIN	TYP (3)	MAX	Units
VDD	Core Supply Voltage		1.14	1.2	1.26	V
VSS	Ground Voltage			0.0		V
VDDA_BIAS_[1:0]	Analog Bias Supply Voltage		1.14	1.2	1.26	V
VDDARX_[3:0] (1)	Analog CML RX Supply Voltage		1.14	1.2	1.26	V
VDDATX_[3:0] (1)	Analog CML TX Supply Voltage		1.14	1.2	1.26	V
VDDRX_[3:0] (1)	CML RX Supply Voltage		1.14	1.2	1.26	V
VDDTX_[3:0] (1)	CML TX Supply Voltage		1.14	1.5	1.89	V
VDD_25	SPI Port Supply Voltage		2.25	2.5	2.75	V
VIN_CML	Input Voltage on any CML pin		0		V_{DDRX}	V
T_C	Case Temperature Range		-55		105	°C
t_R, t_F	Input Rise or Fall time	SPI Port Inputs, (20/80%)			3	ns

Note:

1) There are separate VDDARX, VDDATX, VDDRX, VDDTX pins for each bank. This is indicated by the bus notation suffix: _[3:0]. All four pins for each bank supply are connected to their respective common power supply.

6.0 Electrical Characteristics

6.1 DC Electrical Characteristics

V_{DD}, $V_{DDA\_BIAS\_0,1}$, V_{DDARX}, V_{DDATX}=1.2V±5%, V_{DDRX} =1.2V±5%, V_{DDTX} =1.2V-1.8V±5%, V_{DD_25}=2.5V±10%, -55°C≤T_C≤+105°C, unless otherwise noted.

Table 7: DC Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
VIL	SPI Port: Input Logic Low				0.8	V
VIH	SPI Port: Input Logic High	-	1.7			V
VOL	SPI Port: Output Logic Low	IOL=1mA			0.25	V
VOH	SPI Port: Output Logic High	IOH=1mA	1.9			V
IVDD	Core Supply Current			210	500	mA
IVDDA_BIAS_[1:0]	Analog Bias Voltage Current			7.3	25	mA
IVDDARX_[3:0] (1), (2)	Analog CML RX Supply Current	RX Equalization set to 5'b00000			275	mA
IVDDATX_[3:0] (1), (2)	Analog CML TX Supply Current	TX Drive Current set to 4'b0110			75	mA
IVDDRX_[3:0] (1)	CML Supply RX Current	RX Equalization set to 5'b00000		208	250	mA
IVDDTX_[3:0] (1)	CML Supply TX Current	TX Drive Current set to 4'b0110		208	400	mA
IVDD_25	SPI Port Supply Current			10	350	µA
$P_{D(PWR\_DWN)}$ (3)	Power-Down Power Dissipation			2.4	30	mW
IIL	LVCMOS SPI Input Leakage Current		-1		1	µA
IIL2	CML RX Input Leakage Current		-1		1	µA
IIH	LVCMOS SPI Input Leakage Current		-1		1	µA
IIH2	CML RX Input Leakage Current		-5		5	µA
IOZL	LVCMOS SPI High-Z Output Leakage Current		-1		1	µA
IOZH	LVCMOS SPI High-Z Output Leakage Current		-1		1	µA
QIDD_VDD	Quiescent Current VDD		100		1800	µA
QIDD_VDDA	Quiescent Current VDDA		40		300	µA
QIDD_VDDA_RX_TX	Quiescent Current VDDA_RX_TX		100		800	µA
QIDD_VDDRX	Quiescent Current VDDRX		-60		60	µA
QIDD_VDDTX	Quiescent Current VDDTX		-60		60	µA
QIDD_VDD_25	Quiescent Current VDD_25		50		200	µA

Notes:

1) There are separate VDDARX, VDDATX, VDDRX, VDDTX pins for each bank. This is indicated by the bus notation suffix: _[3:0]. All four pins for each bank supply are connected to their respective common power supply.
2) IVDDARX_[3:0], IVDDATX_[3:0] parameter values are guaranteed by design.
3) Power-down mode: Leakage current only. All circuits powered-down.

6.2 AC Electrical Characteristics

6.2.1 AC Electrical Characteristics: Small & Large Signal Parameters

V_{DD}, $V_{DDA\_BIAS\_0,1}$, V_{DDARX}, V_{DDATX}=1.2V±5%, V_{DDRX} =1.2V±5%, V_{DDTX} =1.2V-1.8V±5%, V_{DD_25}=2.5V±10%, -55°C≤T_C≤+105°C, unless otherwise noted.

Table 8: AC Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
S_{11} (1)	Input Return Loss (RL)	<1.0 GHz			-10	dB
S_{22} (1)	Output Return Loss (RL)	< 1.0 GHz			-10	dB
C_{RX} (1)	RX Pin Capacitance	Zero Bias, f=1MHz			13	pF
C_{TX} (1)	TX Pin Capacitance	Zero Bias, f=1MHz			13	pF
C_{SPI} (1)	SPI Port Pin Capacitance	Zero Bias, f=1MHz			13	pF
VI_CML (2)	Input Amplitude, s.e.	Single Ended, Peak-to-Peak	100		800	mV
VID_CML (2)	Input Amplitude, diff.	Differential, Peak-to-Peak	200		1600	mV
VO_CML (2)	Output Amplitude, s.e.	Single Ended, Peak-to-Peak	200		600	mV
VOD_CML (2)	Output Amplitude, diff.	Differential, Peak-to-Peak	400		1200	mV
$P_{D(TOTAL)}$	Total Power Dissipation	3.125Gbps, All lanes, Full Duplex, Medium CML Drive Strength		1.50	2.2	W

Notes:

1) Determined by characterization.
2) The high-speed I/O are based on current-mode logic (CML) differential (diff.) signaling. Amplitudes are measured from the diff. signals. Single-ended (s.e.) amplitudes are calculated as one-half of the measured diff. signal amplitude.

6.2.2 AC Electrical Characteristics: Timing Parameters

V_{DD}, $V_{DDA\_BIAS\_0,1}$, V_{DDARX}, V_{DDATX}=1.2V±5%, V_{DDRX} =1.2V±5%, V_{DDTX} =1.2V-1.8V±5%, V_{DD_25}=2.5V±10%, -55°C≤T_C≤+105°C, unless otherwise noted.

Table 9: Timing Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
DR (1)	Data Rate / Channel		0.10		3.125	Gbps
t_R, t_F (1)	Output Rise / Fall Time	Differential, 20% - 80%		140		ps
T_J (1), (2)	Total Jitter				40	ps , p-p
f_{CLK}	SPI Clock Frequency	SPI Port			1	MHz
DCR	SPI Clock Duty Cycle Range	SPI Port	40		60	%
t_{SU},t_H	Set Up & Hold Time	SPI Port	10			ns

Notes:

1) Data Rate (DR), Output rise and fall times (t_R, t_F), Total Jitter (T_J): Characterization only.
2) Total Jitter (T_J): Additive DUT jitter. Optimized by adjusting Receiver (RX) Equalization (EQ) setting. The recommended initial RX equalization EQ setting is 5'b10111.

6.3 SPI Port Register Map

Table 10: SPI Port Register Map

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
Reserved			- Reserved	1/0	hex 00	[0:7]
Version Number			Design Version Number - Register ADDRESS hex 01 bits [6:0]. This register ADDRESS is READ ONLY.	1/0	hex 01	[0:6]
POR Flag			The POR Flag is register ADDRESS hex 01, bit [7]. The POR Flag is active high. A POR event sets this flag to logic '1'. All other XPS registers will be initialized (RESET) to their default values. A WRITE to register ADDRESS hex 01 will RESET the POR flag to a logic '0'. All other XPS registers will be RESET to their default values, as defined in this Register Map. For a WRITE to register ADDRESS hex 01, the DATA field values don't matter.	1	hex 01	[7]

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
RLBS0<0>	0	0	Reverse Loop-Back, lane 0, bank 0	0	hex 02	0
RLBS0<1>	1	0	Reverse Loop-Back, lane 1, bank 0	0		1
RLBS0<2>	2	0	Reverse Loop-Back, lane 2, bank 0	0		2
RLBS0<3>	3	0	Reverse Loop-Back, lane 3, bank 0	0		3
RLBS1<0>	0	1	Reverse Loop-Back, lane 0, bank 1	0		4
RLBS1<1>	1	1	Reverse Loop-Back, lane 1, bank 1	0		5
RLBS1<2>	2	1	Reverse Loop-Back, lane 2, bank 1	0		6
RLBS1<3>	3	1	Reverse Loop-Back, lane 3, bank 1	0		7
RLBS2<0>	0	2	Reverse Loop-Back, lane 0, bank 2	0	hex 03	0
RLBS2<1>	1	2	Reverse Loop-Back, lane 1, bank 2	0		1
RLBS2<2>	2	2	Reverse Loop-Back, lane 2, bank 2	0		2
RLBS2<3>	3	2	Reverse Loop-Back, lane 3, bank 2	0		3
RLBS3<0>	0	3	Reverse Loop-Back, lane 0, bank 3	0		4
RLBS3<1>	1	3	Reverse Loop-Back, lane 1, bank 3	0		5
RLBS3<2>	2	3	Reverse Loop-Back, lane 2, bank 3	0		6
RLBS3<3>	3	3	Reverse Loop-Back, lane 3, bank 3	0		7

Note:

1) Reverse Loop-Back (RLB): RLB=0: NOT ACTIVE, RLB=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Bit Number
EQ_0_0<0>	0	0	Receiver post equalization, lane 0, bank 0, bit 0	0	hex 04	0
EQ_0_0<1>	0	0	Receiver post equalization, lane 0, bank 0, bit 1	0		1
EQ_0_0<2>	0	0	Receiver post equalization, lane 0, bank 0, bit 2	0		2
EQ_0_0<3>	0	0	Receiver post equalization, lane 0, bank 0, bit 3	1		3
EQ_0_0<4>	0	0	Receiver post equalization, lane 0, bank 0, bit 4	0		4
EQ_0_1<0>	1	0	Receiver post equalization, lane 1, bank 0, bit 0	0		5
EQ_0_1<1>	1	0	Receiver post equalization, lane 1, bank 0, bit 1	0		6
EQ_0_1<2>	1	0	Receiver post equalization, lane 1, bank 0, bit 2	0		7
EQ_0_1<3>	1	0	Receiver post equalization, lane 1, bank 0, bit 3	1	hex 05	0
EQ_0_1<4>	1	0	Receiver post equalization, lane 1, bank 0, bit 4	0		1
EQ_0_2<0>	2	0	Receiver post equalization, lane 2, bank 0, bit 0	0		2
EQ_0_2<1>	2	0	Receiver post equalization, lane 2, bank 0, bit 1	0		3
EQ_0_2<2>	2	0	Receiver post equalization, lane 2, bank 0, bit 2	0		4
EQ_0_2<3>	2	0	Receiver post equalization, lane 2, bank 0, bit 3	1		5
EQ_0_2<4>	2	0	Receiver post equalization, lane 2, bank 0, bit 4	0		6
EQ_0_3<0>	3	0	Receiver post equalization, lane 3, bank 0, bit 0	0		7
EQ_0_3<1>	3	0	Receiver post equalization, lane 3, bank 0, bit 1	0	hex 06	0
EQ_0_3<2>	3	0	Receiver post equalization, lane 3, bank 0, bit 2	0		1
EQ_0_3<3>	3	0	Receiver post equalization, lane 3, bank 0, bit 3	1		2
EQ_0_3<4>	3	0	Receiver post equalization, lane 3, bank 0, bit 4	0		3
EQ_1_0<0>	0	1	Receiver post equalization, lane 0, bank 1, bit 0	0		4
EQ_1_0<1>	0	1	Receiver post equalization, lane 0, bank 1, bit 1	0		5
EQ_1_0<2>	0	1	Receiver post equalization, lane 0, bank 1, bit 2	0		6
EQ_1_0<3>	0	1	Receiver post equalization, lane 0, bank 1, bit 3	1		7
EQ_1_0<4>	0	1	Receiver post equalization, lane 0, bank 1, bit 4	0	hex 07	0
EQ_1_1<0>	1	1	Receiver post equalization, lane 1, bank 1, bit 0	0		1
EQ_1_1<1>	1	1	Receiver post equalization, lane 1, bank 1, bit 1	0		2
EQ_1_1<2>	1	1	Receiver post equalization, lane 1, bank 1, bit 2	0		3
EQ_1_1<3>	1	1	Receiver post equalization, lane 1, bank 1, bit 3	1		4
EQ_1_1<4>	1	1	Receiver post equalization, lane 1, bank 1, bit 4	0		5
EQ_1_2<0>	2	1	Receiver post equalization, lane 2, bank 1, bit 0	0		6
EQ_1_2<1>	2	1	Receiver post equalization, lane 2, bank 1, bit 1	0		7
EQ_1_2<2>	2	1	Receiver post equalization, lane 2, bank1 , bit 2	0	hex 08	0
EQ_1_2<3>	2	1	Receiver post equalization, lane 2, bank 1, bit 3	1		1
EQ_1_2<4>	2	1	Receiver post equalization, lane 2, bank 1, bit 4	0		2
EQ_1_3<0>	3	1	Receiver post equalization, lane 3, bank 1, bit 0	0		3
EQ_1_3<1>	3	1	Receiver post equalization, lane 3, bank 1, bit 1	0		4
EQ_1_3<2>	3	1	Receiver post equalization, lane 3, bank 1, bit 2	0		5
EQ_1_3<3>	3	1	Receiver post equalization, lane 3, bank 1, bit 3	1		6

EQ_1_3<4>	3	1	Receiver post equalization, lane 3, bank 1, bit 4	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Bit Number
EQ_2_0<0>	0	2	Receiver post equalization, lane 0, bank 2, bit 0	0	hex 09	0
EQ_2_0<1>	0	2	Receiver post equalization, lane 0, bank 2, bit 1	0		1
EQ_2_0<2>	0	2	Receiver post equalization, lane 0, bank 2, bit 2	0		2
EQ_2_0<3>	0	2	Receiver post equalization, lane 0, bank 2, bit 3	1		3
EQ_2_0<4>	0	2	Receiver post equalization, lane 0, bank 2, bit 4	0		4
EQ_2_1<0>	1	2	Receiver post equalization, lane 1, bank 2, bit 0	0		5
EQ_2_1<1>	1	2	Receiver post equalization, lane 1, bank 2, bit 1	0		6
EQ_2_1<2>	1	2	Receiver post equalization, lane 1, bank 2, bit 2	0		7
EQ_2_1<3>	1	2	Receiver post equalization, lane 1, bank 2, bit 3	1	hex 0A	0
EQ_2_1<4>	1	2	Receiver post equalization, lane 1, bank 2, bit 4	0		1
EQ_2_2<0>	2	2	Receiver post equalization, lane 2, bank 2, bit 0	0		2
EQ_2_2<1>	2	2	Receiver post equalization, lane 2, bank 2, bit 1	0		3
EQ_2_2<2>	2	2	Receiver post equalization, lane 2, bank 2, bit 2	0		4
EQ_2_2<3>	2	2	Receiver post equalization, lane 2, bank 2, bit 3	1		5
EQ_2_2<4>	2	2	Receiver post equalization, lane 2, bank 2, bit 4	0		6
EQ_2_3<0>	3	2	Receiver post equalization, lane 3, bank 2, bit 0	0		7
EQ_2_3<1>	3	2	Receiver post equalization, lane 3, bank 2, bit 1	0	hex 0B	0
EQ_2_3<2>	3	2	Receiver post equalization, lane 3, bank 2, bit 2	0		1
EQ_2_3<3>	3	2	Receiver post equalization, lane 3, bank 2, bit 3	1		2
EQ_2_3<4>	3	2	Receiver post equalization, lane 3, bank 2, bit 4	0		3
EQ_3_0<0>	0	3	Receiver post equalization, lane 0, bank 3, bit 0	0		4
EQ_3_0<1>	0	3	Receiver post equalization, lane 0, bank 3, bit 1	0		5
EQ_3_0<2>	0	3	Receiver post equalization, lane 0, bank 3, bit 2	0		6
EQ_3_0<3>	0	3	Receiver post equalization, lane 0, bank 3, bit 3	1		7
EQ_3_0<4>	0	3	Receiver post equalization, lane 0, bank 3, bit 4	0	hex 0C	0
EQ_3_1<0>	1	3	Receiver post equalization, lane 1, bank 3, bit 0	0		1
EQ_3_1<1>	1	3	Receiver post equalization, lane 1, bank 3, bit 1	0		2
EQ_3_1<2>	1	3	Receiver post equalization, lane 1, bank 3, bit 2	0		3
EQ_3_1<3>	1	3	Receiver post equalization, lane 1, bank 3, bit 3	1		4
EQ_3_1<4>	1	3	Receiver post equalization, lane 1, bank 3, bit 4	0		5
EQ_3_2<0>	2	2	Receiver post equalization, lane 2, bank 3, bit 0	0		6
EQ_3_2<1>	2	3	Receiver post equalization, lane 2, bank 3, bit 1	0		7
EQ_3_2<2>	2	3	Receiver post equalization, lane 2, bank 3, bit 2	0	hex 0D	0
EQ_3_2<3>	2	3	Receiver post equalization, lane 2, bank 3, bit 3	1		1
EQ_3_2<4>	2	3	Receiver post equalization, lane 2, bank 3, bit 4	0		2
EQ_3_3<0>	3	3	Receiver post equalization, lane 3, bank 3, bit 0	0		3
EQ_3_3<1>	3	3	Receiver post equalization, lane 3, bank 3, bit 1	0		4
EQ_3_3<2>	3	3	Receiver post equalization, lane 3, bank 3, bit 2	0		5
EQ_3_3<3>	3	3	Receiver post equalization, lane 3, bank 3, bit 3	1		6

EQ_3_3<4>	3	3	Receiver post equalization, lane 3, bank 3, bit 4	0		7

Note:

1) RX Equalization (EQ): See Table 11: Receiver (RX) Post Equalization (EQ) Settings + Figure 13: Receiver (RX) Post Equalization (EQ): Gain (dB) vs. Setting (Hex)

Table 11: Receiver (RX) Post Equalization (EQ) Settings

Setting (HEX)	Gain (dB)	Setting (HEX)	Gain (dB)	Setting (HEX)	Gain (dB)	Setting (HEX)	Gain (dB)
00	-1.4	08	11.8	10	26.6	18	33.7
01	-1.6	09	14.6	11	27.8	19	34.4
02	-1.5	0A	16.7	12	28.9	1A	35.0
03	-0.9	0B	19.2	13	30.0	1B	35.6
04	0.5	0C	20.9	14	30.8	1C	36.1
05	3.3	0D	22.7	15	31.7	1D	36.6
06	6.4	0E	24.2	16	32.5	1E	37.1
07	9.7	0F	25.7	17	33.2	1F	37.6

Notes:

1) Determined by simulation. Nominal values.
2) Gain (dB) at Nyquist frequency (1.5625 GHz).

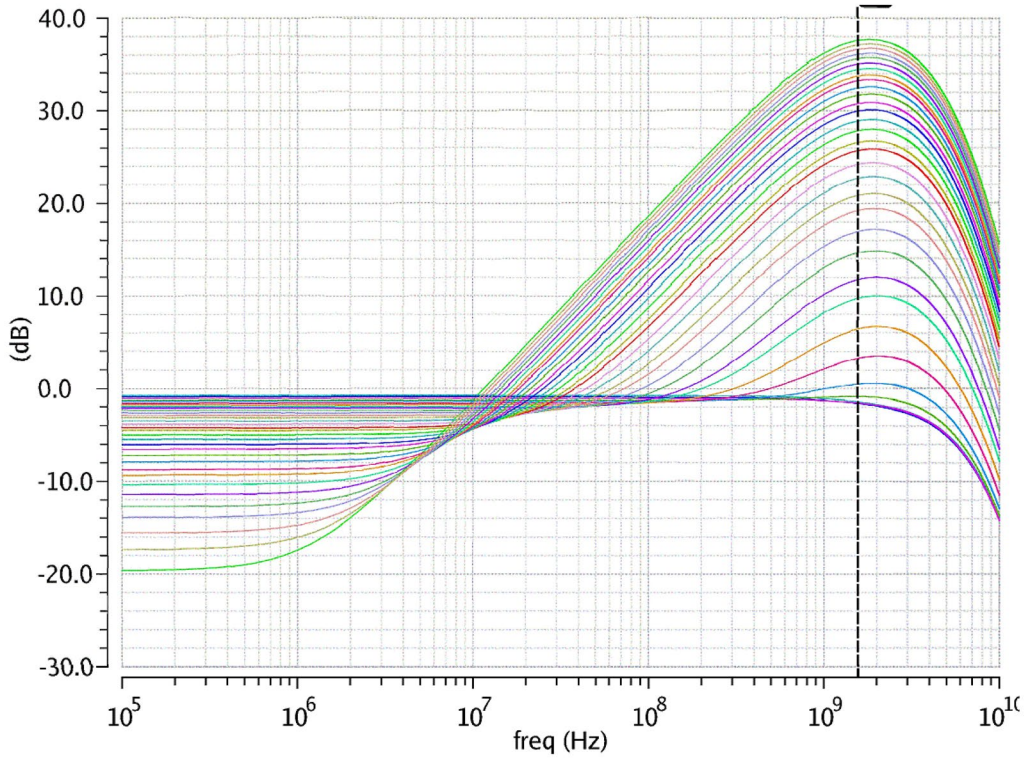

Figure 13: Receiver (RX) Post Equalization (EQ): Gain (dB) vs. Setting (Hex)

Table 10: SPI Port Register Map (Continued)

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
PD_rx_0<0>	0	0	Receiver Power Down lane 0, bank 0	0	hex 0E	0
PD_rx_0<1>	1	0	Receiver Power Down lane 1, bank 0	0		1
PD_rx_0<2>	2	0	Receiver Power Down lane 2, bank 0	0		2
PD_rx_0<3>	3	0	Receiver Power Down lane 3, bank 0	0		3
PD_rx_1<0>	0	1	Receiver Power Down lane 0, bank 1	0		4
PD_rx_1<1>	1	1	Receiver Power Down lane 1, bank 1	0		5
PD_rx_1<2>	2	1	Receiver Power Down lane 2, bank 1	0		6
PD_rx_1<3>	3	1	Receiver Power Down lane 3, bank 1	0		7
PD_rx_2<0>	0	2	Receiver Power Down lane 0, bank 2	0	hex 0F	0
PD_rx_2<1>	1	2	Receiver Power Down lane 1, bank 2	0		1
PD_rx_2<2>	2	2	Receiver Power Down lane 2, bank 2	0		2
PD_rx_2<3>	3	2	Receiver Power Down lane 3, bank 2	0		3
PD_rx_3<0>	0	3	Receiver Power Down lane 0, bank 3	0		4
PD_rx_3<1>	1	3	Receiver Power Down lane 1, bank 3	0		5
PD_rx_3<2>	2	3	Receiver Power Down lane 2, bank 3	0		6
PD_rx_3<3>	3	3	Receiver Power Down lane 3, bank 3	0		7

Note:

1) RX Power Down (PD): PD=0: INACTIVE, PD=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Bit Number
HI_Z_TX_0<0>	0	0	Transmitter termination High Z, lane 0, bank 0	0	hex 10	0
HI_Z_TX_0<1>	1	0	Transmitter termination High Z, lane 1, bank 0	0		1
HI_Z_TX_0<2>	2	0	Transmitter termination High Z, lane 2, bank 0	0		2
HI_Z_TX_0<3>	3	0	Transmitter termination High Z, lane 3, bank 0	0		3
HI_Z_TX_0<4>	0	1	Transmitter termination High Z, lane 0, bank 1	0		4
HI_Z_TX_0<5>	1	1	Transmitter termination High Z, lane 1, bank 1	0		5
HI_Z_TX_0<6>	2	1	Transmitter termination High Z, lane 2, bank 1	0		6
HI_Z_TX_0<7>	3	1	Transmitter termination High Z, lane 3, bank 1	0		7
HI_Z_TX_1<0>	0	2	Transmitter termination High Z, lane 0, bank 2	0	hex 11	0
HI_Z_TX_1<1>	1	2	Transmitter termination High Z, lane 1, bank 2	0		1
HI_Z_TX_1<2>	2	2	Transmitter termination High Z, lane 2, bank 2	0		2
HI_Z_TX_1<3>	3	2	Transmitter termination High Z, lane 3, bank 2	0		3
HI_Z_TX_1<4>	0	3	Transmitter termination High Z, lane 0, bank 3	0		4
HI_Z_TX_1<5>	1	3	Transmitter termination High Z, lane 1, bank 3	0		5
HI_Z_TX_1<6>	2	3	Transmitter termination High Z, lane 2, bank 3	0		6
HI_Z_TX_1<7>	3	3	Transmitter termination High Z, lane 3, bank 3	0		7

Note:

1) TX HIGH-Z (HI-Z): HI-Z=0: INACTIVE, HI-Z=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
HI_Z_RX0<0>	0	0	Receiver termination High Z, lane 0, bank 0	0	hex 12	0
HI_Z_RX0<1>	1	0	Receiver termination High Z, lane 1, bank 0	0		1
HI_Z_RX0<2>	2	0	Receiver termination High Z, lane 2, bank 0	0		2
HI_Z_RX0<3>	3	0	Receiver termination High Z, lane 3, bank 0	0		3
HI_Z_RX1<0>	0	1	Receiver termination High Z, lane 0, bank 1	0		4
HI_Z_RX1<1>	1	1	Receiver termination High Z, lane 1, bank 1	0		5
HI_Z_RX1<2>	2	1	Receiver termination High Z, lane 2, bank 1	0		6
HI_Z_RX1<3>	3	1	Receiver termination High Z, lane 3, bank 1	0		7
HI_Z_RX2<0>	0	2	Receiver termination High Z, lane 0, bank 2	0	hex 13	0
HI_Z_RX2<1>	1	2	Receiver termination High Z, lane 1, bank 2	0		1
HI_Z_RX2<2>	2	2	Receiver termination High Z, lane 2, bank 2	0		2
HI_Z_RX2<3>	3	2	Receiver termination High Z, lane 3, bank 2	0		3
HI_Z_RX3<0>	0	3	Receiver termination High Z, lane 0, bank 3	0		4
HI_Z_RX3<1>	1	3	Receiver termination High Z, lane 1, bank 3	0		5
HI_Z_RX3<2>	2	3	Receiver termination High Z, lane 2, bank 3	0		6
HI_Z_RX3<3>	3	3	Receiver termination High Z, lane 3, bank 3	0		7

Note:

1) RX HIGH-Z (HI-Z): HI-Z=0: INACTIVE, HI-Z=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
EN_LOS_0<0>	0	0	Lane 0 enable loss of signal detector, bank 0	0	hex 14	0
EN_LOS_0<1>	1	0	Lane 1 enable loss of signal detector, bank 0	0		1
EN_LOS_0<2>	2	0	Lane 2 enable loss of signal detector, bank 0	0		2
EN_LOS_0<3>	3	0	Lane 3 enable loss of signal detector, bank 0	0		3
EN_LOS_1<0>	0	1	Lane 0 enable loss of signal detector, bank 1	0		4
EN_LOS_1<1>	1	1	Lane 1 enable loss of signal detector, bank 1	0		5
EN_LOS_1<2>	2	1	Lane 2 enable loss of signal detector, bank 1	0		6
EN_LOS_1<3>	3	1	Lane 3 enable loss of signal detector, bank 1	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
EN_LOS_2<0>	0	2	Lane 0 enable loss of signal detector, bank 2	0	hex 15	0
EN_LOS_2<1>	1	2	Lane 1 enable loss of signal detector, bank 2	0		1
EN_LOS_2<2>	2	2	Lane 2 enable loss of signal detector, bank 2	0		2
EN_LOS_2<3>	3	2	Lane 3 enable loss of signal detector, bank 2	0		3
EN_LOS_3<0>	0	3	Lane 0 enable loss of signal detector, bank 3	0		4
EN_LOS_3<1>	1	3	Lane 1 enable loss of signal detector, bank 3	0		5
EN_LOS_3<2>	2	3	Lane 2 enable loss of signal detector, bank 3	0		6
EN_LOS_3<3>	3	3	Lane 3 enable loss of signal detector, bank 3	0		7

Note:

1) Loss of Signal (LOS): LOS=0: INACTIVE, LOS=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
TX_I_0<0>	0	0	Lane 0 transmitter drive current, bank 0, bit 0	0	hex 16	0
TX_I_0<1>	0	0	Lane 0 transmitter drive current, bank 0, bit 1	0		1
TX_I_0<2>	0	0	Lane 0 transmitter drive current, bank 0, bit 2	0		2
TX_I_0<3>	0	0	Lane 0 transmitter drive current, bank 0, bit 3	1		3
TX_I_0<4>	1	0	Lane 1 transmitter drive current, bank 0, bit 0	0		4
TX_I_0<5>	1	0	Lane 1 transmitter drive current, bank 0, bit 1	0		5
TX_I_0<6>	1	0	Lane 1 transmitter drive current, bank 0, bit 2	0		6
TX_I_0<7>	1	0	Lane 1 transmitter drive current, bank 0, bit 3	1		7
TX_I_0<8>	2	0	Lane 2 transmitter drive current, bank 0, bit 0	0	hex 17	0
TX_I_0<9>	2	0	Lane 2 transmitter drive current, bank 0, bit 1	0		1
TX_I_0<10>	2	0	Lane 2 transmitter drive current, bank 0, bit 2	0		2
TX_I_0<11>	2	0	Lane 2 transmitter drive current, bank 0, bit 3	1		3
TX_I_0<12>	3	0	Lane 3 transmitter drive current, bank 0, bit 0	0		4
TX_I_0<13>	3	0	Lane 3 transmitter drive current, bank 0, bit 1	0		5
TX_I_0<14>	3	0	Lane 3 transmitter drive current, bank 0, bit 2	0		6
TX_I_0<15>	3	0	Lane 3 transmitter drive current, bank 0, bit 3	1		7
TX_I_0<16>	0	1	Lane 0 transmitter drive current, bank 1, bit 0	0	hex 18	0
TX_I_0<17>	0	1	Lane 0 transmitter drive current, bank 1, bit 1	0		1
TX_I_0<18>	0	1	Lane 0 transmitter drive current, bank 1, bit 2	0		2
TX_I_0<19>	0	1	Lane 0 transmitter drive current, bank 1, bit 3	1		3
TX_I_0<20>	1	1	Lane 1 transmitter drive current, bank 1, bit 0	0		4
TX_I_0<21>	1	1	Lane 1 transmitter drive current, bank 1, bit 1	0		5
TX_I_0<22>	1	1	Lane 1 transmitter drive current, bank 1, bit 2	0		6
TX_I_0<23>	1	1	Lane 1 transmitter drive current, bank 1, bit 3	1		7
TX_I_0<24>	2	1	Lane 2 transmitter drive current, bank 1, bit 0	0	hex 19	0
TX_I_0<25>	2	1	Lane 2 transmitter drive current, bank 1, bit 1	0		1
TX_I_0<26>	2	1	Lane 2 transmitter drive current, bank 1, bit 2	0		2
TX_I_0<27>	2	1	Lane 2 transmitter drive current, bank 1, bit 3	1		3
TX_I_0<28>	3	1	Lane 3 transmitter drive current, bank 1, bit 0	0		4
TX_I_0<29>	3	1	Lane 3 transmitter drive current, bank 1, bit 1	0		5
TX_I_0<30>	3	1	Lane 3 transmitter drive current, bank 1, bit 2	0		6
TX_I_0<31>	3	1	Lane 3 transmitter drive current, bank 1, bit 3	1		7
TX_I_1<0>	0	2	Lane 0 transmitter drive current, bank 2, bit 0	0	hex 1A	0
TX_I_1<1>	0	2	Lane 0 transmitter drive current, bank 2, bit 1	0		1
TX_I_1<2>	0	2	Lane 0 transmitter drive current, bank 2, bit 2	0		2
TX_I_1<3>	0	2	Lane 0 transmitter drive current, bank 2, bit 3	1		3
TX_I_1<4>	1	2	Lane 1 transmitter drive current, bank 2, bit 0	0		4
TX_I_1<5>	1	2	Lane 1 transmitter drive current, bank 2, bit 1	0		5
TX_I_1<6>	1	2	Lane 1 transmitter drive current, bank 2, bit 2	0		6
TX_I_1<7>	1	2	Lane 1 transmitter drive current, bank 2, bit 3	1		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
TX_I_1<8>	2	2	Lane 2 transmitter drive current, bank 2, bit 0	0	hex 1B	0
TX_I_1<9>	2	2	Lane 2 transmitter drive current, bank 2, bit 1	0		1
TX_I_1<10>	2	2	Lane 2 transmitter drive current, bank 2, bit 2	0		2
TX_I_1<11>	2	2	Lane 2 transmitter drive current, bank 2, bit 3	1		3
TX_I_1<12>	3	2	Lane 3 transmitter drive current, bank 2, bit 0	0		4
TX_I_1<13>	3	2	Lane 3 transmitter drive current, bank 2, bit 1	0		5
TX_I_1<14>	3	2	Lane 3 transmitter drive current, bank 2, bit 2	0		6
TX_I_1<15>	3	2	Lane 3 transmitter drive current, bank 2, bit 3	1		7
TX_I_1<16>	0	3	Lane 0 transmitter drive current, bank 3, bit 0	0	hex 1C	0
TX_I_1<17>	0	3	Lane 0 transmitter drive current, bank 3, bit 1	0		1
TX_I_1<18>	0	3	Lane 0 transmitter drive current, bank 3, bit 2	0		2
TX_I_1<19>	0	3	Lane 0 transmitter drive current, bank 3, bit 3	1		3
TX_I_1<20>	1	3	Lane 1 transmitter drive current, bank 3, bit 0	0		4
TX_I_1<21>	1	3	Lane 1 transmitter drive current, bank 3, bit 1	0		5
TX_I_1<22>	1	3	Lane 1 transmitter drive current, bank 3, bit 2	0		6
TX_I_1<23>	1	3	Lane 1 transmitter drive current, bank 3, bit 3	1		7
TX_I_1<24>	2	3	Lane 2 transmitter drive current, bank 3, bit 0	0	hex 1D	0
TX_I_1<25>	2	3	Lane 2 transmitter drive current, bank 3, bit 1	0		1
TX_I_1<26>	2	3	Lane 2 transmitter drive current, bank 3, bit 2	0		2
TX_I_1<27>	2	3	Lane 2 transmitter drive current, bank 3, bit 3	1		3
TX_I_1<28>	3	3	Lane 3 transmitter drive current, bank 3, bit 0	0		4
TX_I_1<29>	3	3	Lane 3 transmitter drive current, bank 3, bit 1	0		5
TX_I_1<30>	3	3	Lane 3 transmitter drive current, bank 3, bit 2	0		6
TX_I_1<31>	3	3	Lane 3 transmitter drive current, bank 3, bit 3	1		7

Note:

1) TX Drive Current (TX-I): See Table 12: Transmitter (TX) I(VDDTX), VOD_CML vs. I(TX) [3:0] Setting

Table 12: Transmitter (TX) I(VDDTX), VOD_CML vs. I(TX) [3:0] Setting

I(TX) [3:0]	I(VDDTX) (mA)	ΔI (mA)	RL=50||50=25Ω Vout (s.e.) (Vp-p)	RL=50||50=25Ω Vout (diff.) (Vp-p)
0	7.6	-	0.19	0.38
1	9.76	2.16	0.24	0.49
2	11.7	1.94	0.29	0.59
3	13.76	2.06	0.34	0.69
4	15.31	1.55	0.38	0.77
5	17.29	1.98	0.43	0.86
6	19.05	1.76	0.48	0.95
7	20.92	1.87	0.52	1.05
8	21.96	1.04	0.55	1.10
9	23.71	1.75	0.59	1.19
10	25.23	1.52	0.63	1.26
11	26.80	1.57	0.67	1.34
12	27.93	1.13	0.70	1.40
13	29.32	1.39	0.73	1.47
14	30.50	1.18	0.76	1.53
15	31.70	1.20	0.79	1.59

Note:

1) Determined by simulation. Nominal values.

Table 13: Transmitter (TX) I(VDDTX), VOD_CML vs. VDDTX

I(TX) [3:0] (hex)	VDD=VDDRX (V)	VDDTX (V)	I(VDDTX) (mA)	VOD_CML (mV p-p diff.)
8	1.2	1.2	39	870
8	1.2	1.3	39	890
8	1.2	1.4	40	900
8	1.2	1.5	40	900
8	1.2	1.6	40	900
8	1.2	1.7	40	900
8	1.2	1.8	40	900
8	1.2	1.9	40	900
8	1.2	1.8	40	900
A	1.2	1.8	43	1020
B	1.2	1.8	45	1080
C	1.2	1.8	46	1140
D	1.2	1.8	48	1190
E	1.2	1.8	49	1210
F	1.2	1.8	50	1240

Notes:

1) Determined by measurement. Nominal values.
2) PRBS 2^7-1; 100 Mbps

Table 10: SPI Port Register Map (Continued)

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
PD_TX_0<0>	0	0	Power down transmitter, lane 0, bank 0	0	hex 1E	0
PD_TX_0<1>	1	0	Power down transmitter, lane 1, bank 0	0		1
PD_TX_0<2>	2	0	Power down transmitter, lane 2, bank 0	0		2
PD_TX_0<3>	3	0	Power down transmitter, lane 3, bank 0	0		3
PD_TX_0<4>	0	1	Power down transmitter, lane 0, bank 1	0		4
PD_TX_0<5>	1	1	Power down transmitter, lane 1, bank 1	0		5
PD_TX_0<6>	2	1	Power down transmitter, lane 2, bank 1	0		6
PD_TX_0<7>	3	1	Power down transmitter, lane 3, bank 1	0		7
PD_TX_1<0>	0	2	Power down transmitter, lane 0, bank 2	0	hex 1F	0
PD_TX_1<1>	1	2	Power down transmitter, lane 1, bank 2	0		1
PD_TX_1<2>	2	2	Power down transmitter, lane 2, bank 2	0		2
PD_TX_1<3>	3	2	Power down transmitter, lane 3, bank 2	0		3
PD_TX_1<4>	0	3	Power down transmitter, lane 0, bank 3	0		4
PD_TX_1<5>	1	3	Power down transmitter, lane 1, bank 3	0		5
PD_TX_1<6>	2	3	Power down transmitter, lane 2, bank 3	0		6
PD_TX_1<7>	3	3	Power down transmitter, lane 3, bank 3	0		7

Note:

1) TX Power Down (PD): PD=0: INACTIVE, PD=1: ACTIVE

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
PDR0<0>	0	0	Power down receiver bias current, lane 0, bank 0	0	hex 20	0
PDR0<1>	1	0	Power down receiver bias current, lane 1, bank 0	0		1
PDR0<2>	2	0	Power down receiver bias current, lane 2, bank 0	0		2
PDR0<3>	3	0	Power down receiver bias current, lane 3, bank 0	0		3
PDR0<4>	0	1	Power down receiver bias current, lane 0, bank 1	0		4
PDR0<5>	1	1	Power down receiver bias current, lane 1, bank 1	0		5
PDR0<6>	2	1	Power down receiver bias current, lane 2, bank 1	0		6
PDR0<7>	3	1	Power down receiver bias current, lane 3, bank 1	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
PDR1<0>	0	2	Power down receiver bias current, lane 0, bank 2	0	hex 21	0
PDR1<1>	1	2	Power down receiver bias current, lane 1, bank 2	0		1
PDR1<2>	2	2	Power down receiver bias current, lane 2, bank 2	0		2
PDR1<3>	3	2	Power down receiver bias current, lane 3, bank 2	0		3
PDR1<4>	0	3	Power down receiver bias current, lane 0, bank 3	0		4
PDR1<5>	1	3	Power down receiver bias current, lane 1, bank 3	0		5
PDR1<6>	2	3	Power down receiver bias current, lane 2, bank 3	0		6
PDR1<7>	3	3	Power down receiver bias current, lane 3, bank 3	0		7

Note:

1) RX Bias Current Power Down (PD): PD=0: INACTIVE, PD=1: ACTIVE

Table 10: SPI Port Register Map (Continued)

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
S_ab0<0>	0	0	Multiplexer control, side a to side b, lane 0, bank 0	0	hex 22	0
S_ab0<1>	1	0	Multiplexer control, side a to side b, lane 1, bank 0	0		1
S_ab0<2>	2	0	Multiplexer control, side a to side b, lane 2, bank 0	0		2
S_ab0<3>	3	0	Multiplexer control, side a to side b, lane 3, bank 0	0		3
S_ab1<0>	0	1	Multiplexer control, side a to side b, lane 0, bank 1	0		4
S_ab1<1>	1	1	Multiplexer control, side a to side b, lane 1, bank 1	0		5
S_ab1<2>	2	1	Multiplexer control, side a to side b, lane 2, bank 1	0		6
S_ab1<3>	3	1	Multiplexer control, side a to side b, lane 3, bank 1	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
S_ba2<0>	0	2	Multiplexer control, side b to side a, lane 0, bank 2	0	hex 23	0
S_ba2<1>	1	2	Multiplexer control, side b to side a, lane 1, bank 2	0		1
S_ba2<2>	2	2	Multiplexer control, side b to side a, lane 2, bank 2	0		2
S_ba2<3>	3	2	Multiplexer control, side b to side a, lane 3, bank 2	0		3
S_ba3<0>	0	3	Multiplexer control, side b to side a, lane 0, bank 3	0		4
S_ba3<1>	1	3	Multiplexer control, side b to side a, lane 1, bank 3	0		5
S_ba3<2>	2	3	Multiplexer control, side b to side a, lane 2, bank 3	0		6
S_ba3<3>	3	3	Multiplexer control, side b to side a, lane 3, bank 3	0		7

Note:
Multiplexer Control (MUX-CTRL): See Figure 14: XPS Multiplexer Switch Connections; Table 14: XPS MUX Decoder Settings – See Figures 1, 14

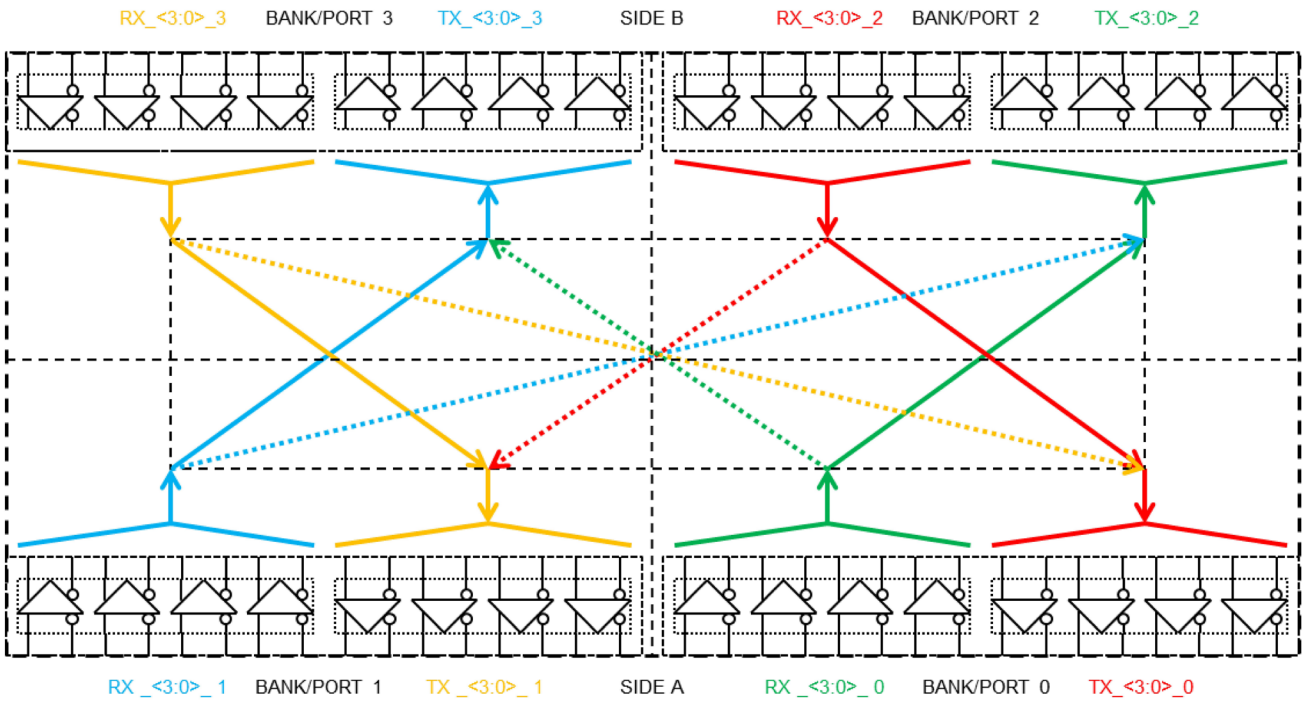

Figure 14: XPS Multiplexer Switch Connections

Notes:

1) BANK ORIENTATION = PACKAGE TOP VIEW
2) <RX/TX>_<CHANNEL#>_<BANK/PORT#>
3) SOLID LINES = DEFAULT CONNECTIONS
4) DASHED LINES = OPTIONAL CONNECTIONS

Table 14: XPS MUX Decoder Settings – See Figures 1, 14

Received Data Paths to Bank 0

Setting Identifier	Multiplexer	Bit Value	Data Source	Data Destination
0a	S_ba2_<0>	0	RX Bank 2, Lane 0	TX Bank 0, Lane 0
0b	S_ba2_<0>	1	RX Bank 3, Lane 0	TX Bank 0, Lane 0
1a	S_ba2_<1>	0	RX Bank 2, Lane 1	TX Bank 0, Lane 1
1b	S_ba2_<1>	1	RX Bank 3, Lane 1	TX Bank 0, Lane 1
2a	S_ba2_<2>	0	RX Bank 2, Lane 2	TX Bank 0, Lane 2
2b	S_ba2_<2>	1	RX Bank 3, Lane 2	TX Bank 0, Lane 2
3a	S_ba2_<3>	0	RX Bank 2, Lane 3	TX Bank 0, Lane 3
3b	S_ba2_<3>	1	RX Bank 3, Lane 3	TX Bank 0, Lane 3

Received Data Paths to Bank 1

Setting Identifier	Multiplexer	Bit Value	Data Source	Data Destination
0a	S_ba3_<0>	0	RX Bank 3, Lane 0	TX Bank 1, Lane 0
0b	S_ba3_<0>	1	RX Bank 2, Lane 0	TX Bank 1, Lane 0
1a	S_ba3_<1>	0	RX Bank 3, Lane 1	TX Bank 1, Lane 1
1b	S_ba3_<1>	1	RX Bank 2, Lane 1	TX Bank 1, Lane 1
2a	S_ba3_<2>	0	RX Bank 3, Lane 2	TX Bank 1, Lane 2
2b	S_ba3_<2>	1	RX Bank 2, Lane 2	TX Bank 1, Lane 2
3a	S_ba3_<3>	0	RX Bank 3, Lane 3	TX Bank 1, Lane 3
3b	S_ba3_<3>	1	RX Bank 2, Lane 3	TX Bank 1, Lane 3

Received Data Paths to Bank 2

Setting Identifier	Multiplexer	Bit Value	Data Source	Data Destination
0a	S_ab0_<0>	0	RX Bank 0, Lane 0	TX Bank 2, Lane 0
0b	S_ab0_<0>	1	RX Bank 1, Lane 0	TX Bank 2, Lane 0
1a	S_ab0_<1>	0	RX Bank 0, Lane 1	TX Bank 2, Lane 1
1b	S_ab0_<1>	1	RX Bank 1, Lane 1	TX Bank 2, Lane 1
2a	S_ab0_<2>	0	RX Bank 0, Lane 2	TX Bank 2, Lane 2
2b	S_ab0_<2>	1	RX Bank 1, Lane 2	TX Bank 2, Lane 2
3a	S_ab0_<3>	0	RX Bank 0, Lane 3	TX Bank 2, Lane 3
3b	S_ab0_<3>	1	RX Bank 1, Lane 3	TX Bank 2, Lane 3

Received Data Paths to Bank 3

Setting Identifier	Multiplexer	Bit Value	Data Source	Data Destination
0a	S_ab1_<0>	0	RX Bank 1, Lane 0	TX Bank 3, Lane 0
0b	S_ab1_<0>	1	RX Bank 0, Lane 0	TX Bank 3, Lane 0
1a	S_ab1_<1>	0	RX Bank 1, Lane 1	TX Bank 3, Lane 1
1b	S_ab1_<1>	1	RX Bank 0, Lane 1	TX Bank 3, Lane 1
2a	S_ab1_<2>	0	RX Bank 1, Lane 2	TX Bank 3, Lane 2
2b	S_ab1_<2>	1	RX Bank 0, Lane 2	TX Bank 3, Lane 2
3a	S_ab1_<3>	0	RX Bank 1, Lane 3	TX Bank 3, Lane 3
3b	S_ab1_<3>	1	RX Bank 0, Lane 3	TX Bank 3, Lane 3

Table 10: SPI Port Register Map (Continued)

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
RT<0>	All	All	Termination resistance trim bit 0	1	hex 24	0
RT<1>	All	All	Termination resistance trim bit 1	1		1
PD_all_bias	All	All	Power down all bias generators	0		2
PD_mux	All	All	Power down all reverse loop back multiplexers	0		3
PD_XP<0>		Note 1	Power down cross point multiplexer 0	0		4
PD_XP<1>		Note 1	Power down cross point multiplexer 1	0		5
PD_XP<2>		Note 1	Power down cross point multiplexer 2	0		6
PD_XP<3>		Note 1	Power down cross point multiplexer 3	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
PD_XP<4>		Note 1	Power down cross point multiplexer 4	0	hex 25	0
PD_XP<5>		Note 1	Power down cross point multiplexer 5	0		1
PD_XP<6>		Note 1	Power down cross point multiplexer 6	0		2
PD_XP<7>		Note 1	Power down cross point multiplexer 7	0		3
SPARE_0				0		4
SPARE_1				1		5
Read_ Addressed_ Registers			Logic '1': A SPI-READ will read the registers at the addresses, regardless of whether or not the internal register values have been updated to the outputs that control the analog- functions or not. Logic '0': A SPI-READ will read the register bits that actively control the analog function blocks.	0	hex 25	6
Update _All_ Control_Regis ters			Logic '1': SPI-WRITE will update all of the XPS addressed register bits. These register bits control the analog functions. A SPI-READ of this register bit will return a logic '0' always, since it is self-clearing. Both *Read_Addressed_Registers and Update_All_Control_Registers* are written simultaneously when logic '1'.	0	hex 25	7

Notes:

1) PD<7:0> must be 0 for any operational configuration except a part-wide power-down
2) All XPS Registers: Active High: 0: INACTIVE, 1: ACTIVE
3) XPS Bank Power Down (PD): PD=0: INACTIVE, PD=1: ACTIVE

Table 10: SPI Port Register Map (Continued)

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
SPARE_2			Unused	1	hex 26	0
SPARE_3			Unused	0		1
SPARE_4			Unused	1		2
SPARE_5			Unused	0		3
SPARE_6			Unused	1		4
SPARE_7			Unused	0		5
SPARE_8			Unused	1		6
SPARE_9			Unused	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
LOS_0<0>	0	0	Loss of Signal (LOS) Status Bit - READ ONLY	0	hex 27	0
LOS_0<1>	1	0	Loss of Signal (LOS) Status Bit - READ ONLY	0		1
LOS_0<2>	2	0	Loss of Signal (LOS) Status Bit - READ ONLY	0		2
LOS_0<3>	3	0	Loss of Signal (LOS) Status Bit - READ ONLY	0		3
LOS_1<0>	0	1	Loss of Signal (LOS) Status Bit - READ ONLY	0		4
LOS_1<1>	1	1	Loss of Signal (LOS) Status Bit - READ ONLY	0		5
LOS_1<2>	2	1	Loss of Signal (LOS) Status Bit - READ ONLY	0		6
LOS_1<3>	3	1	Loss of Signal (LOS) Status Bit - READ ONLY	0		7

Name	Lane	Bank	Function	Initial Condition (1/ 0)	Register Address	Register Bit
LOS_2<0>	0	2	Loss of Signal (LOS) Status Bit - READ ONLY	0	hex 28	0
LOS_2<1>	1	2	Loss of Signal (LOS) Status Bit - READ ONLY	0		1
LOS_2<2>	2	2	Loss of Signal (LOS) Status Bit - READ ONLY	0		2
LOS_2<3>	3	2	Loss of Signal (LOS) Status Bit - READ ONLY	0		3
LOS_3<0>	0	3	Loss of Signal (LOS) Status Bit - READ ONLY	0		4
LOS_3<1>	1	3	Loss of Signal (LOS) Status Bit - READ ONLY	0		5
LOS_3<2>	2	3	Loss of Signal (LOS) Status Bit - READ ONLY	0		6
LOS_3<3>	3	3	Loss of Signal (LOS) Status Bit - READ ONLY	0		7

Note:

1) Loss of Signal (LOS) Status Bit (Flag): LOS: 0: INACTIVE, 1: ACTIVE - READ ONLY

7.0 Package Drawings

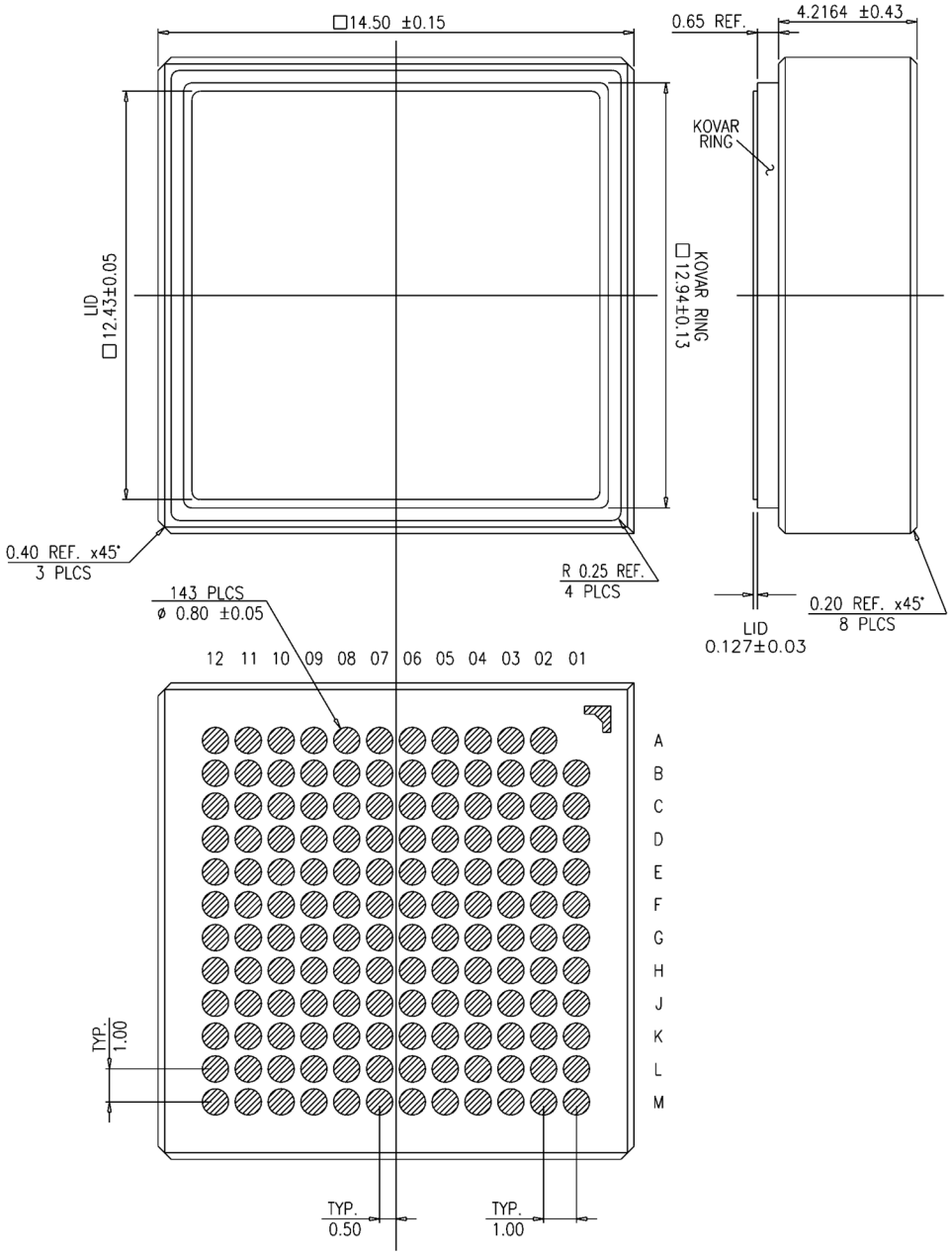

Figure 13a: 143 Land, Ceramic Land Grid Array (CLGA)

Notes:

1) Units are millimeters
2) The package lid is connected To VSS
3) Exposed-metal plating per MIL-PRF-38535
   All: Electrolytic Nickel 2.54-8.89um
   Top-Side: Immersion Gold 0.03-0.10um
   Bottom-Side: Electrolytic Gold 2.54-5.72um.
4) Tolerance is ±0.13 where not otherwise stated. This includes "TYP" dimensions.

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7.0 Package Drawings (Continued)

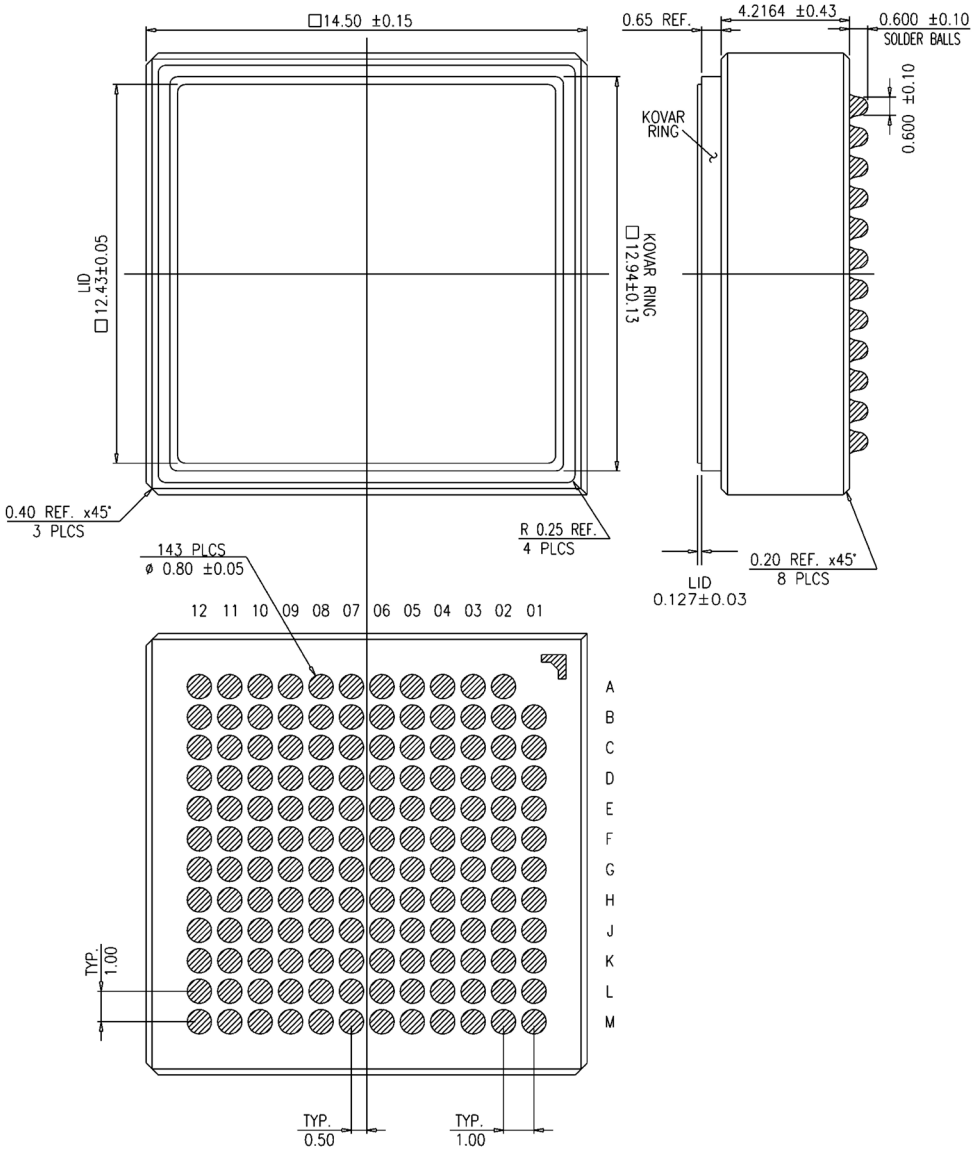

Figure 13b: 143 Ball, Ceramic Ball Grid Array (CBGA)

Notes:

1) Units are millimeters
2) The package lid is connected To VSS
3) Exposed-metal plating per MIL-PRF-38535
   All: Electrolytic Nickel 2.54-8.89um
   Top-Side: Immersion Gold 0.03-0.10um
   Bottom-Side: Electrolytic Gold 2.54-5.72um.
4) Tolerance is ±0.13 where not otherwise stated. This includes "TYP" dimensions.
5) Solder balls are available for Prototypes and Engineering samples only, as they are not QML-qualified.
6) The dimensions shown for the attached solder balls are approximate.

7.0 Package Drawings (Continued)

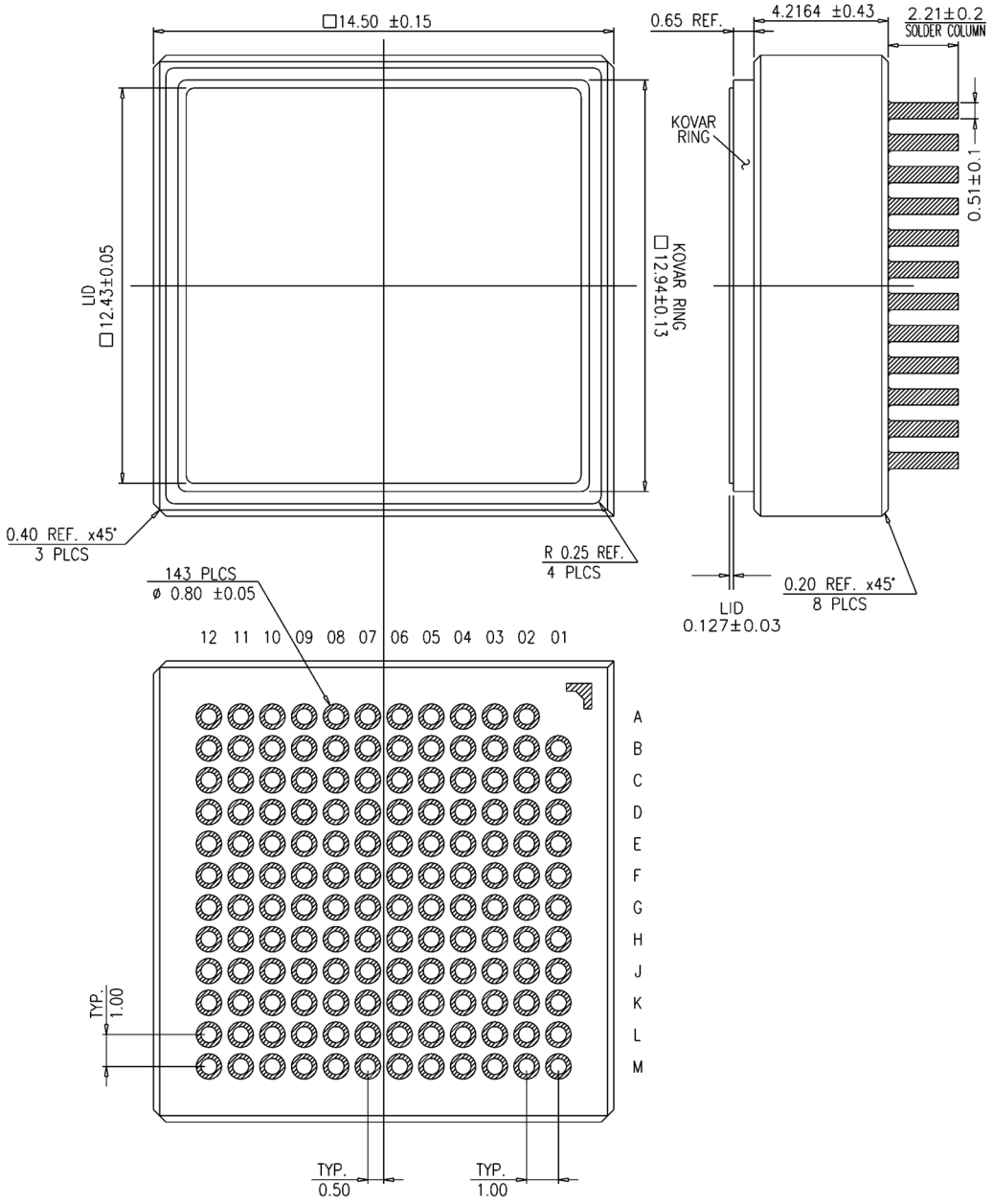

Figure 13c: 143 Column, Ceramic Column Grid Array (CCGA)

Notes:

1) Units are millimeters
2) The package lid is connected to VSS
3) Exposed-metal plating per MIL-PRF-38535
   All: Electrolytic Nickel 2.54-8.89um
   Top-Side: Immersion Gold 0.03-0.10um
   Bottom-Side: Electrolytic Gold 2.54-5.72um.
4) Tolerance is ±0.13 where not otherwise stated. This Includes "TYP" Dimensions.

3.125 Gbps Crosspoint Switch (XPS)

UT65CML8X8FD

8.0 Ordering Information

8.1 CAES Part Number Ordering Information

Datasheet Part Numbering

UT65CML8X8FD * * * *

Lead Finish: (Notes: 1)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Screening Level: (Notes: 2, 3, 4)
(P) = Prototype Flow (Temperature Range: 25°C only)
(F) = HiRel Flow (Temperature Range: -55°C to +105°C)

Case Outline: (Note: 5, 6, 7)
(Z) = 143-Land Ceramic Land Grid Array (CLGA)
(C) = 143-Ball Ceramic Ball Grid Array (CBGA)
(S) = 143-Column Ceramic Column Grid Array (CCGA)

Part Type:
(-) = None

Part Number: 65CML8X8FD 3.125 Gbps 8x8 Crosspoint Switch (XPS)

Notes:

1) Lead finish (A, C, or F) must be specified.
2) Prototype Flow per CAES Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
3) HiRel Flow per CAES Manufacturing Flows Document. Radiation TID tolerance may (or may not) be ordered.
4) Contact factory to define alternative screening options.
5) For ceramic Land Grid Array (LGA) package, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) package, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) package, the lead finish is "F" (Solder Column).
6) Ball Grid Array (BGA) Case Outline is only available for Prototype Flow Screening Level. (BGA Case Outline is not available for HiRel Flow Screening Level.)
7) All Case Outline options (i.e. LGA, BGA, CGA) are available for Prototype Flow Screening Level.

3.125 Gbps Crosspoint Switch (XPS)

UT65CML8X8FD

8.2 SMD Part Number Ordering Information

SMD Part Numbering

5962 * 17213 ** * * *

Lead Finish: (Notes: 1)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(F) = Solder Column (Copper wound, solder coated)

Case Outline: (Note: 2)
(X) = Ceramic Land Grid Array (CLGA)
(Y) = Ceramic Column Grid Array (CCGA)

QML/JAN Class: (Note: 3)
(Q) = Class Q
(V) = Class V

Device Type: (Note: 4)
(01) = UT65CML8X8FD (QML-Q, V)
(02) = UT65CML8X8FD (QML-Q+)

SMD Project Number:
(17213) = 3.125 Gbps 8x8 Crosspoint Switch (XPS)

Radiation Hardness Assurance: (Notes: 5, 6)
(R) = 100 krad(Si)

Federal Stock Class Designator

Notes:

1) Lead finish must be specified. Part marking will reflect the lead finish applied to the device shipped.
2) For ceramic Land Grid Array (LGA) packages, the lead finish is "C" (Gold-only). For Ball Grid Arrays (BGA) packages, the lead finish is "A" (Hot Solder Dipped). For Column Grid Array (CGA) packages, the lead finish is "F" (Solder Column).
3) Contact factory to determine alternative screening options.
4) CAES Q+ flow, as defined in Section 4.2.1f of the SMD, provides QML-Q product through the SMD that is manufactured with CAES standard QML-V flow
5) A radiation hardness assurance level must be selected. The use of "-" indicates no radiation hardness assurance guarantee.
6) Device type 01 is irradiated at dose rate = 50 – 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment.

DATASHEET

RELEASED 03/23/22

9.0 Revision History

Date	Revision	Change Description
2017-11-01	2.0.0	Advanced Datasheet – Draft – Correction to Ordering Info., pp. 40, 41.
2018-03-21	2.0.1	Advanced Datasheet – Draft – Edits for uniform header size
2018-03-22	2.0.2	Advanced Datasheet – Draft – Updates to Electrical Tables 4, 6, 7, 8
2018-04-10	2.0.3	Advanced Datasheet – Draft – Update to Table 5: Added SEU parameter, + formatting
2018-04-12	2.0.4	Adv. D.S., Draft: 1.4.6,7-SPI; 3,5,6.2.1-P_D, Tables 4, 6, 8; 6.1-MAXtoTYP, Table 7
2018-04-17	2.0.5	Adv. D.S., Draft: 6.1, Table 7; 6.2.1, Table 8; 6.2.2 Table 9: Notes updated
2018-07-16	2.0.6	Adv. D.S. to Prelim. D.S.
2018-08-15	2.0.7	Tables 2, 4, 6, 7, p. 13, 18, 19, 20: V_{DD} parameter name; Table 7, p. 20: Conditions
2018-11-26	2.0.8	Tables 4,6: Thermal properties updates; Tables 4, 6, 8: Footnotes updates
2019-01-24	2.0.9	1.4 SPI Port: p.8
2019-02-14	2.0.10	Table 8, p. 21: Added pin capacitance
2019-03-12	2.1.0	Global DS change: T_C max. from 110°C to 105°C
2019-06-19	2.1.1	Added Note 6, p.40: Ball Grid Array (BGA) package is only available for Prototype Screening Level
2020-03-25	2.1.2	Updates and corrections from Product Owner DS review comments
2020-04-21	2.1.3	Updates to Tables 4, 6, p. 18, 19: T_C, T_J, T_{STG}; Table 7, p. 20: device operating current, including IVDDARX,TX_[3:0]
2020-05-07	2.1.4	Updates to Tables 4, 8, p.18, 21: P_D max., $P_{D(TOTAL)}$ max. thermal parameters.
2020-05-19	2.1.5	Updates to Table 5, p. 19: Conditions
2020-06-11	2.1.6	Updates to Section 4, Table 5, p. 19: Parameters + limits
2020-07-01	2.1.7	Figure 1, p.3: SPI Port signal names updated
2020-07-14	2.1.8	Section 8.2 SMD P/N Ordering Info., p.39: SMD Part No.: Added QML-Q+ Option
2020-07-21	2.1.9	Section 8.1, p.40: CAES P/N Ordering Info.: HiRel Flow: Letter "C" to "F"
2020-08-04	2.2.0	Section 7.0, p.37-39: Package drawings update: Added Note 4, package tolerance
2020-10-21	2.2.1	Section 6.1, Table 7, p.19: Added Input Leakage Current Parameters, x6
2020-11-03	2.2.2	Section 1.3, p.6: Correction: VO/VOD_CML: 600/1200mV max.; See Table 8, p. 20; Table 7, p.19: I/O Leakage Current: Added pin details and conditions.
2020-12-02	2.2.3	Section 6.1, Table 7, p.19: Updates to current parameter values
2022-02-15	2.2.4	AMR Table, p.18: Update to T_J, T_{STG} thermal parameters.
2022-03-23	2.2.5	Table 2, p.14: Pin List – Pin Description, Table 3, p.17: Pin List / Package Config., Correction: G11=TXP_3_3, G12=TXN_3_3

3.125 Gbps Crosspoint Switch (XPS)

UT65CML8X8FD

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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