DATASHEET

RELEASED 12/20

16Megabit Non-Volatile MRAM

UT8MR2M8

Features

- Single 3.3-V power supply read/write
- Fast 45ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- Equal address and chip-enable access times
- HiRel temperature range (-40°C to 105°C)
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data retention: 20 years (-40°C to 105°C)
- Read/write endurance: unlimited for 20 years (-40°C to 105°C)
- Operational environment:
  - Total dose: 1 Mrad(Si)
  - SEL Immune: 112 MeV-cm^2/mg @125°C
  - SEU Immune: Memory Cell 112 MeV-cm^2/mg @25°C
- Two 40-pin package options available
- Standard Microelectronics Drawing 5962-12227
  - QML Q, Q+ and V

Introduction

The CAES 16Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory compatible with traditional asynchronous SRAM operations, organized as 2,097,152 words by 8bits.

The MRAM is equipped with chip enable (/E), write enable (/W), and output enable (/G) pins, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 20-year retention at temperature and data is automatically protected against power loss by a low voltage write inhibit.

The 16Mb MRAM is designed specifically for operation in HiRel environments. As shown in Table 3, the magneto-resistive bit cells are immune to Single Event Effects (SEE). To guard against transient effects, an Error Correction Code (ECC) is included within the device. ECC check bits are generated and stored within the MRAM array during writes. If a single bit error is found during a read cycle, it is automatically corrected in the data presented to the user.

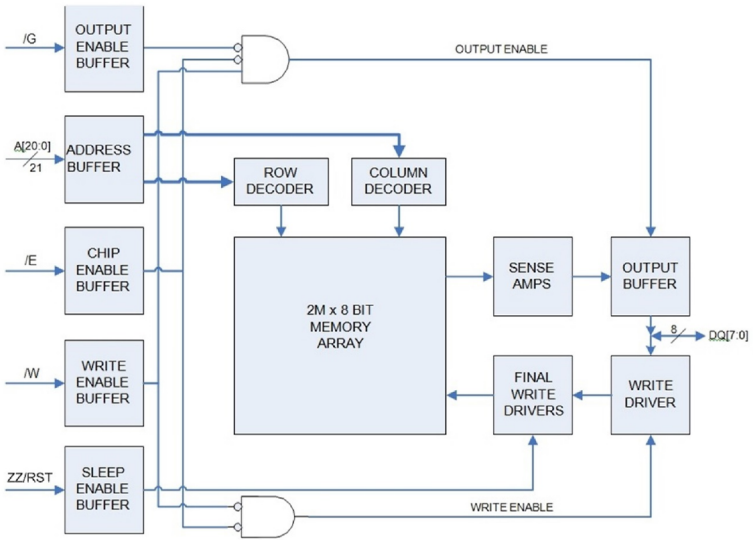


Figure 1. UT8MR2M8 MRAM Block Diagram

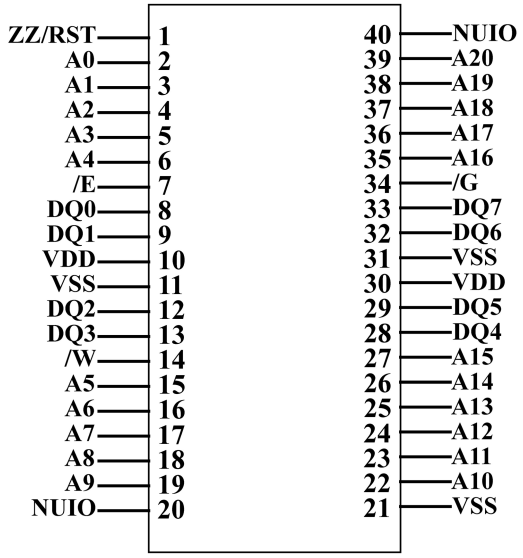


Figure 2. Package (X) 40-lead CFP-50 Mil Pitch

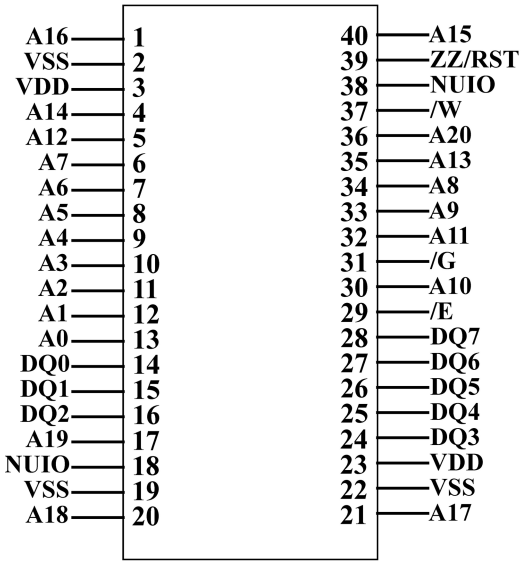


Figure 3. Package (Y) 40-lead CFP-25 Mil Pitch

Pin Names

Table 1. 2M x 8 Pin Functions

Signal Name	Function
A[20:0]	Address Input
/E	Chip Enable
/W	Write Enable
/G	Output Enable
DQ[7:0]	Data I/O
VDD	Power Supply
VSS	Ground
ZZ/RST	Deep Power Down/ Reset (Internal pull down)
NUIO	Not used input/output Recommend tie low

Device Operation

The UT8MR2M8 has four control inputs called Chip Enable (/E), Write Enable (/W), Output Enable (/G) and Sleep/Reset Mode (ZZ/RST); 21 address inputs, A[20:0]; and eight bidirectional data lines, DQ[7:0]. /E controls device selection, active, and standby modes. Asserting /E enables the device, causes I_{DD} to rise to its active value, and decodes the 21 address inputs to select one of 2,097,152 words in the memory. /W controls read and write operations. During a read cycle, /G must be asserted to enable the outputs. ZZ/RST controls the sleep/reset mode operation and provides device reset capability. Enabling sleep/reset mode causes all other inputs to be don't cares. The following descriptions assume that sleep/reset mode is disabled when ZZ/RST is logic low.

Table 2. Device Operation Truth Table

ZZ/ Reset	/E	/G	/W	Mode	VDD Current	DQ[7:0]
H	X	X	X	Deep Sleep/ Reset Mode	Q_{IZZ}	HI-Z
L	H	X	X	Not Selected	Q_{IDD}	HI-Z
L	L	H	H	Output Disabled	I_{DDR}	HI-Z
L	L	L	H	Byte Read	I_{DDR}	D_{OUT}
L	L	X	L	Byte Write	I_{DDW}	D_{IN}

Read Cycle

A combination of /W greater than V_{IH} (min) and /E less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

MRAM Read Cycle 1, the Address Access in Figure 5a, is initiated by a change in address inputs while the chip is enabled with /G asserted and /W deasserted. Valid data appears on data outputs DQ[7:0] after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

MRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5b, is initiated by /E going active while /G remains asserted, /W remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight-bit word addressed by A[20:0] is accessed and appears at the data outputs DQ[7:0].

Write Cycle

A combination of /W and /E less than V_{IL}(max) defines a write cycle. The state of /G is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either /G is greater than V_{IH}(min), or when /W is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 6a, is defined by a write terminated by /W going high, with /E still active. The write pulse width is defined by t_{WLWH} when the write is initiated by /W, and by t_{WLEH} when the write is initiated by /E. Unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 6b, is defined by a write terminated by /E going inactive. The write pulse width is defined by t_{ELWH} when the write is initiated by /W, and by t_{ELEH} when the write is initiated by /E going active. For the /E initiated write, unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

Operational Environment

The UT8MR2M8 MRAM incorporates special design and layout features which allows operation in harsh environments.

Table 3. Operational Environment Design Specifications

Parameter	Limit	Units
TID	1	Mrad(Si)
SEL Immunity [1]	≤ 112	MeV-cm²/mg
SEU Memory Cell Immunity [2]	≤ 112	MeV-cm²/mg

Notes:
1) SEL test performance at V_{DD} = 3.6V and temperature= 125°C.
2) SEU test performance at V_{DD} = 3.0V and unpowered at room temperature.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The /E and /W control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so the signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /E and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

The MRAM supports sleep/reset mode operation using the ZZ/ RST control pin. To enter sleep/reset mode, ZZ/RST must be pulled high. The device will enter sleep/reset mode within 40ns. In order to exit sleep/reset mode, /E and /W must be high before ZZ/RST is pulled low. As soon as ZZ/RST is driven low, the user must allow 100us before performing any other operation in order for the device to properly initialize. CAES recommends designing a system level method to toggle the ZZ/RST pin in order to reset the MRAM device.

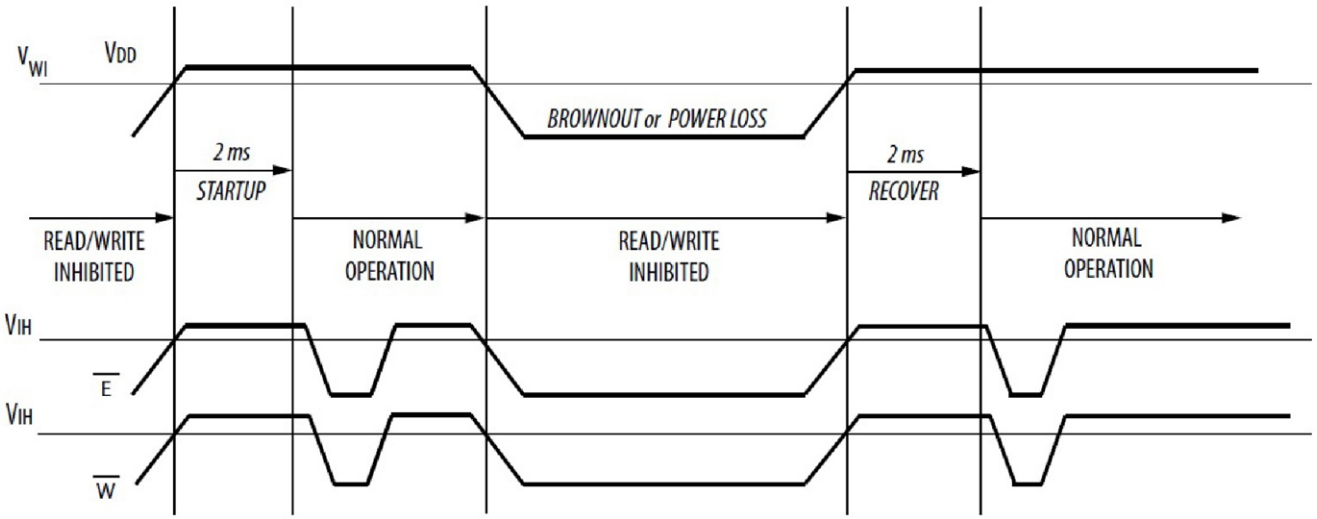


Figure 4. UT8MR2M8 Power Up and Power Down Sequencing Diagram

16Megabit Non-Volatile MRAM

UT8MR2M8

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

The device contains protection against magnetic fields. Precautions should be taken to avoid device exposure of any magnetic field intensity greater than specified.

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage [2]	-0.5 to 4.3	V
V_{IN}	Voltage on any pin [2]	-0.5 to V_{DD}+0.5	V
I_{IO}	DC I/O current per pin @ T_J = 125° for 20yrs	± 20	mA
P_D	Package power dissipation permitted [3]	9	W
T_J	Maximum junction temperature	+150	°C
Θ_{JC}	Thermal resistance junction to case	5	°C/W
T_{STG}	Storage temperature	-65 to +125	°C
ESD_{HBM}	ESD (Class 2)	2000	V
H_{max_write}	Maximum magnetic field during write	8000	A/m
H_{max_read}	Maximum magnetic field during read or standby	8000	A/m

Notes:

1) Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2) All voltages are referenced to V_{SS}.
3) Per MIL-STD-883, Method 1012, Section 3.4.1 $P_D = \frac{(TJ(max) - T_C(max))}{\Theta_{JC}}$

Recommended Operating Conditions

Symbol	Parameter	Limits
T_C	Operating case temperature	-40 to +105°C
V_{DD}	Operating supply voltage	3.0V to 3.6V
V_{WI}	Write inhibit voltage	2.5V to 3.0V [1]
V_{IH}	Input high voltage	2.0V to V_{DD}+0.3V
V_{IL}	Input low voltage	V_{SS} -0.3V to 0.8V

Notes:

1) After power up or if V_{DD} falls below V_{WI}, a waiting period of 2 ms must be observed, and /E and /W must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI}.
2) The MRAM is guaranteed to activate write inhibit below 2.5V, but may enter inhibit mode anywhere within this voltage range. It is guaranteed to exit write inhibit mode once recommended operating voltage range is reached.

DC Electrical Characteristics (Pre and Post-Radiation) *

V_{DD} = 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered [5]

Symbol	Parameter	Condition		MIN	MAX	Unit
V_{IH}	High-level input voltage			2.0		V
V_{IL}	Low-level input voltage				0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 4mA,V_{DD} =V_{DD} (min)			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} =+100μA,V_{DD} =V_{DD} (min)			V_{SS}+0.2	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA,V_{DD} =V_{DD} (min)		2.4		V
V_{OH2}	High-level output voltage	I_{OH} = -100μA,V_{DD} =V_{DD} (min)		V_{DD}-0.2		V
C_{IN} [1]	Input capacitance (Applies to A[20:0])	f = 1MHz @ 0V			12	pF
C_{IO} [1]	Bidirectional I/O capacitance	f = 1MHz @ 0V			14	pF
C_{IO2} [1]	Package X Bidirectional I/O capacitance (applies to DQ[7:0])	f = 1MHz @ 0V			10	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}		-1	+1	μA
I_{INZZ}	Input leakage current ZZ/RST	V_{IN} = V_{DD} and V_{SS}			±100	μA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS}, V_{DD} = V_{DD} (max) /G = V_{DD} (max)		-1	+1	μA
I_{OS} [2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O =V_{DD} V_{DD} = V_{DD} (max), V_O = V_{SS}		-100	+100	mA
I_{DDR}	Active read supply current	Read mode f =MAX (I_{OUT}=0mA; V_{DD} =max)			110	mA
I_{DDW}	Active write supply current	Write mode f =10 MHz (V_{DD} = max)			110	mA
Q_{IDD}	Quiescent supply current	CMOS leakage current (/E and /W = V_{DD}; all other inputs equal V_{SS} or V_{DD}; V_{DD} = max)	-40°C and +25°C		11	mA
			+105°C		20	mA
Q_{IZZ} [4]	Deep power down and reset supply current	CMOS leakage current (/E, /W, ZZ = V_{DD}; all other inputs equal V_{SS} or V_{DD}; V_{DD} = max)			1	mA

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2) Guaranteed by design.
3) Not more than one output may be shorted at a time for maximum duration of one second.
4) Allow 100μs to exit sleep/reset mode before performing any other operation and observe start up time and start up conditions for /W and /E.
5) Testing performed with Error Correction Code Enabled (ECC-ON), customer use case always utilizes ECC-ON.

AC Characteristics Read Cycle [1] (Pre and Post-Radiation) *

V_{DD} = 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered [5]

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV}	Read cycle time	45		ns
t_{AVQV}	Address access time		45	ns
t_{ELQV} [2]	Enable access time		45	ns
t_{GLQV} [3]	Output enable access time		22	ns
t_{AXQX}	Output hold from address change	3		ns
t_{ELQX} [4]	Enable low to output active	3		ns
t_{GLQX} [4]	Output enable low to output active	0		ns
t_{EHQZ} [4]	Enable high to output Hi-Z	0	15	ns
t_{GHQZ} [4]	Output enable high to output Hi-Z	0	10	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) /W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2) Address valid before or at the same time /E goes low.
3) t_{GLQV} output enable valid time unless t_{AVAV} or t_{AVQV} have not been satisfied.
4) Transition is measured at +/-400mV from the steady-state voltage.
5) Testing performed with Error Correction Code Enabled (ECC-ON), customer use case always utilizes ECC-ON

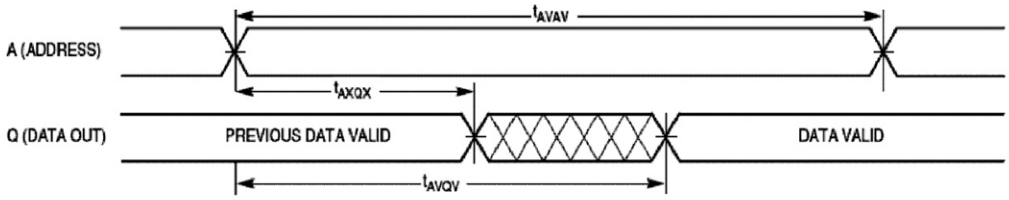


Figure 5a. MRAM Read Cycle 1

Note:

1) Devices is continuously selected (/E≤ V_{IL}, /G≤V_{IL}).

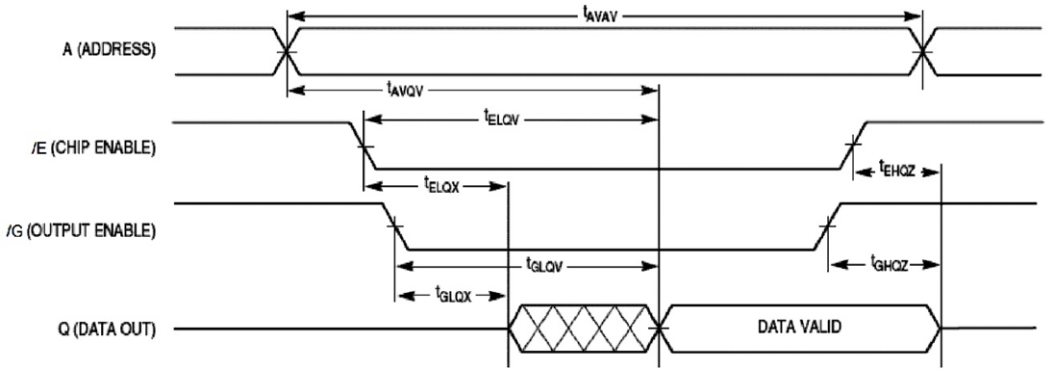


Figure 5b. MRAM Read Cycle 2

AC Characteristics /W Controlled Write Cycle (Pre and Post-Radiation) *

V_{DD}= 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered [4]

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV} [2]	Write cycle time	45		ns
t_{AVWL}	Address set-up time	0		ns
t_{AVWH}	Address valid to end of write (/G high)	28		ns
t_{AVWH}	Address valid to end of write (/G low)	28		
t_{WLWH} t_{WLEH}	Write pulse width (/G high or low)	28		ns
t_{DVWH}	Data valid to end of write	10		ns
t_{WHDX}	Data hold time	0		ns
t_{WLQZ} [3]	Write low to data Hi-Z	0	15	ns
t_{WHQX} [3]	Write high to output active	3		ns
t_{WHAX}	Write recovery time	16		ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) All write occurs during the overlap of /E low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2) All write cycle timings are referenced from the last valid address to the first transition address.
3) Transition is measured +/-400mV from the steady-state voltage.
4) Testing performed with Error Correction Code Enabled (ECC-ON), customer use case always utilizes ECC-ON

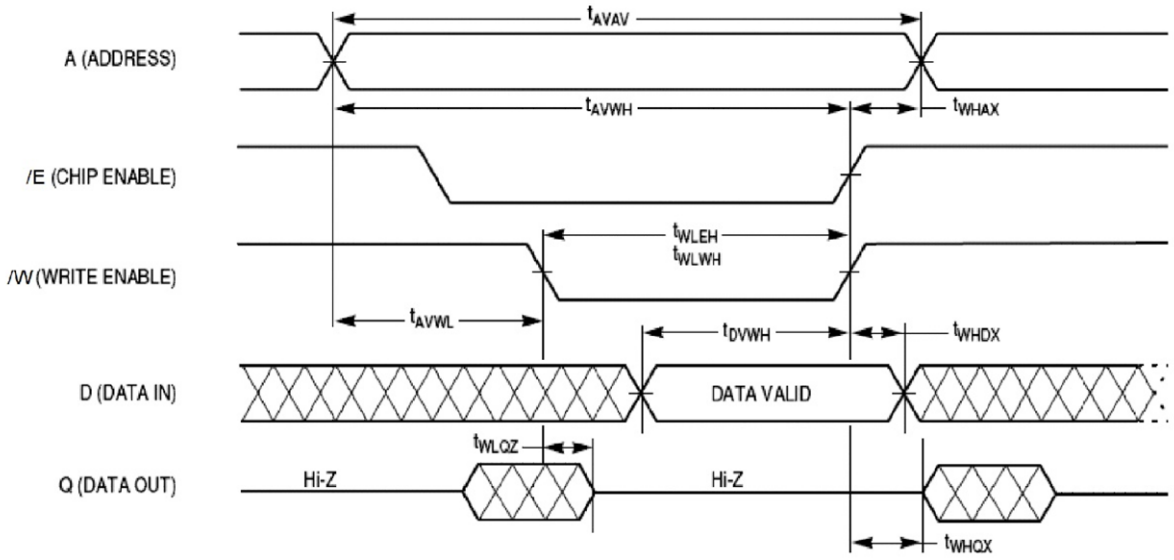


Figure 6a. MRAM Write Cycle 1 (/W Controlled Access)

AC Characteristics /E Controlled Write Cycle [1] (Pre and Post-Radiation) *

V_{DD}= 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered [4]

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV} [2]	Write cycle time	45		ns
t_{AVEL}	Address set-up time	0		ns
t_{AVEH}	Address valid to end of write (/G high)	28		ns
t_{AVEH}	Address valid to end of write (/G low)	28		
t_{ELEH} t_{ELWH}	Enable to end of write (/G high)	28		ns
t_{ELEH} [3] t_{ELWH} [3]	Enable to end of write (/G low)	28		ns
t_{DVEH}	Data valid to end of write	10		ns
t_{EHDX}	Data hold time	0		ns
t_{EHAX}	Write recovery time	16		ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) All write occurs during the overlap of /E low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
2) All write cycle timings are referenced from the last valid address to the first transition address.
3) If /E goes low at the same time or after /W goes low, the output will remain in a high-impedance state. If /E goes high at the same time or before /W goes high, the output will remain in a high-impedance state.
4) Testing performed with Error Correction Code Enabled (ECC-ON), customer use case always utilizes ECC-ON

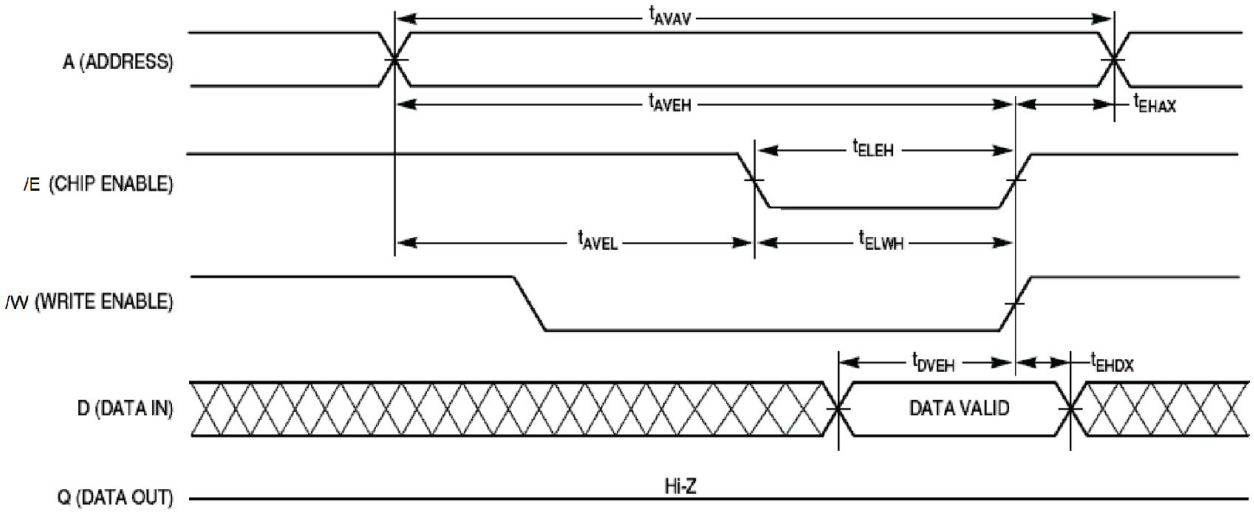


Figure 6b. MRAM Write Cycle 2 (/E Controlled)

AC Characteristics Sleep/Reset Mode (Pre and Post-Radiation) *

V_{DD}= 3.0V to 3.6V; Unless otherwise noted, Tc is per the temperature ordered [4]

Symbol	Parameter	MIN	MAX	Unit
t_{ZZL} [1, 3]	Sleep/reset mode exit delay		100	µs
t_{ZZH} [2, 3]	Sleep/reset mode access time	45		ns
t_{EZZ} [3]	Sleep/reset mode exit setup time	0		ns
t_{ZZS} [3]	Sleep/reset mode settle time		200	µs

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL – STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) /E and /W must be high when ZZ/RST is pulled low and remain high during t_{ZZL} in order to exit sleep/reset mode.
2) ZZ/RST must be high for 40ns in order to enter sleep/reset mode.
3) Guaranteed by design.
4) Testing performed with Error Correction Code Enabled (ECC-ON), customer use case always utilizes ECC-ON

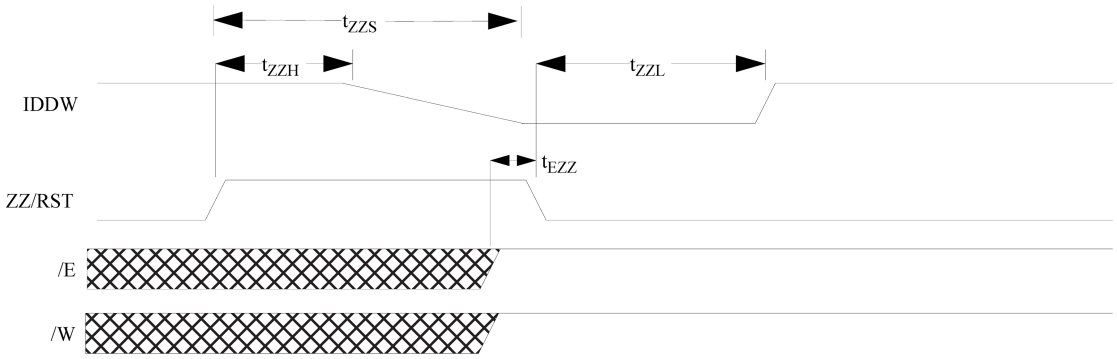


Figure 7. MRAM Sleep/Reset Mode Timing Diagram

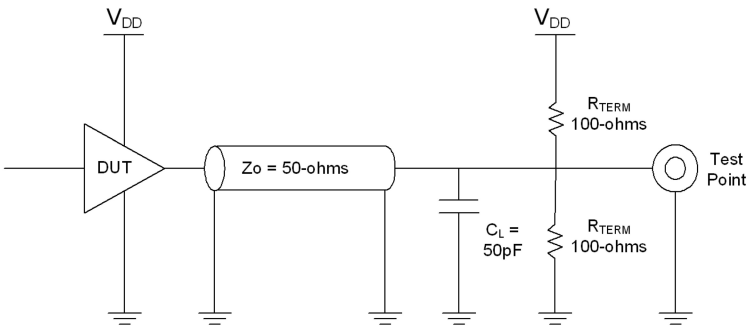


Figure 8. AC Output Test Load or Equivalent

Note:

1) Measurement of data output occurs at the low to high or high to low transition mid-point, typically, V_{DD}/2.

Packages

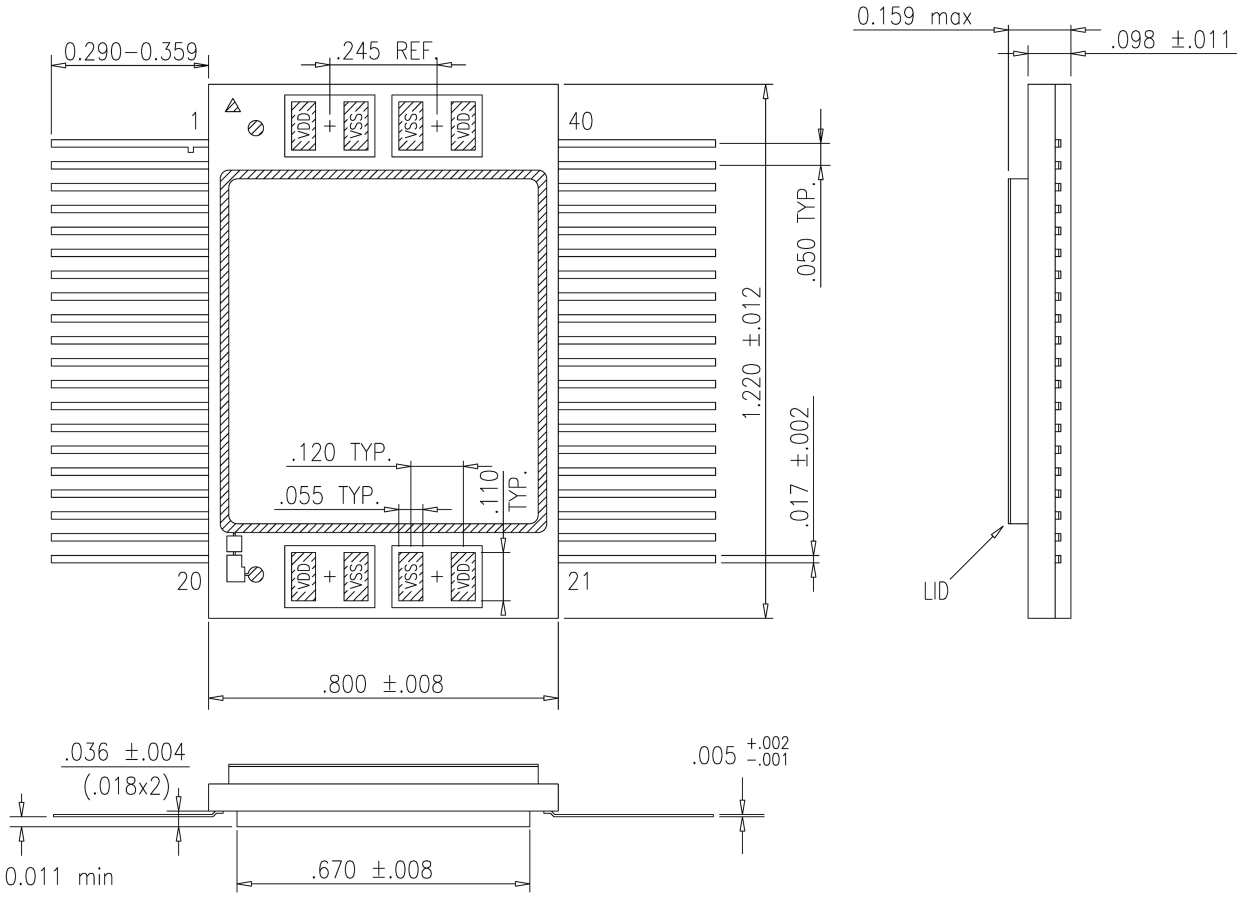


Figure 9. Package Option X 40-Pin Ceramic Flatpack - 50 Mil Pitch

Notes:

1) Lid is connected to VSS
2) Units are in inches

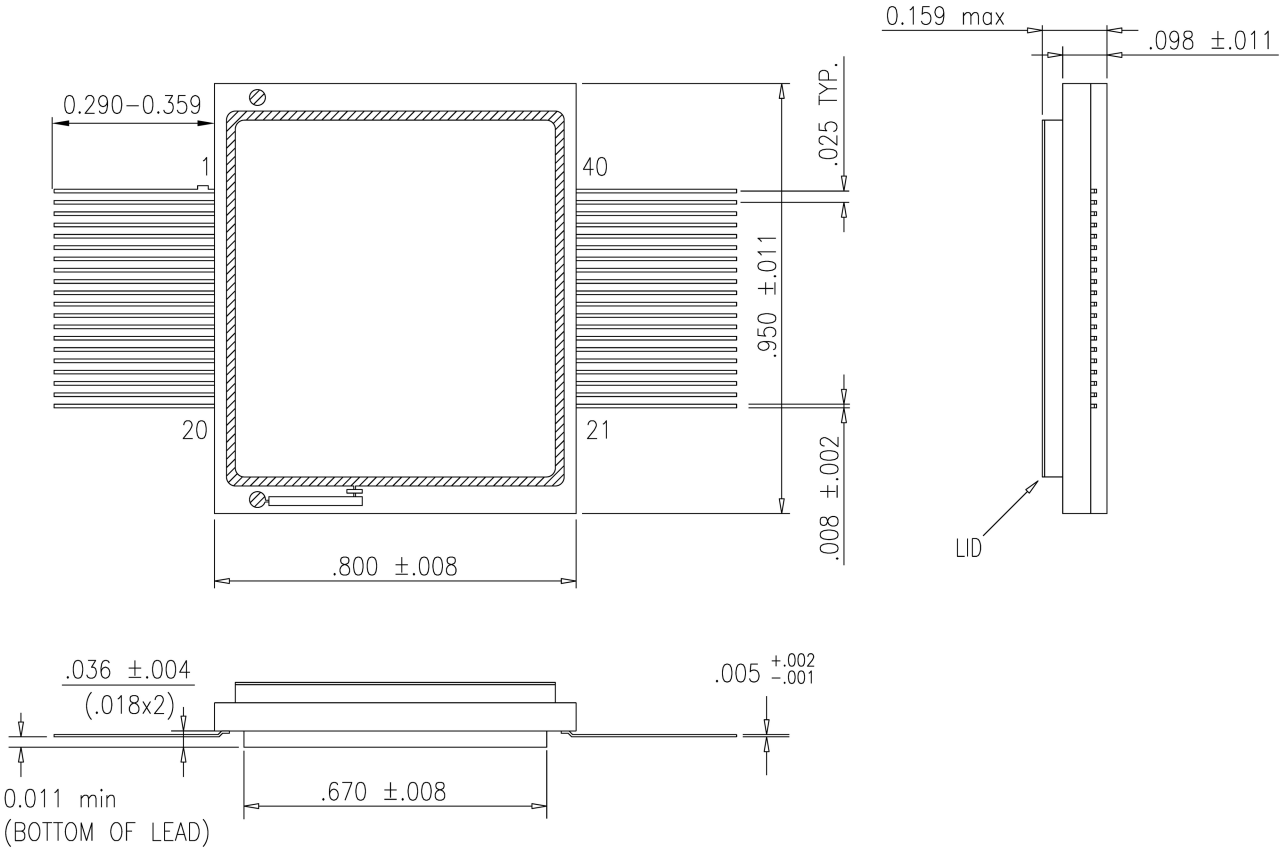


Figure 10. Package Option Y 40-Pin Ceramic Flatpack - 25 Mil Pitch

Notes:

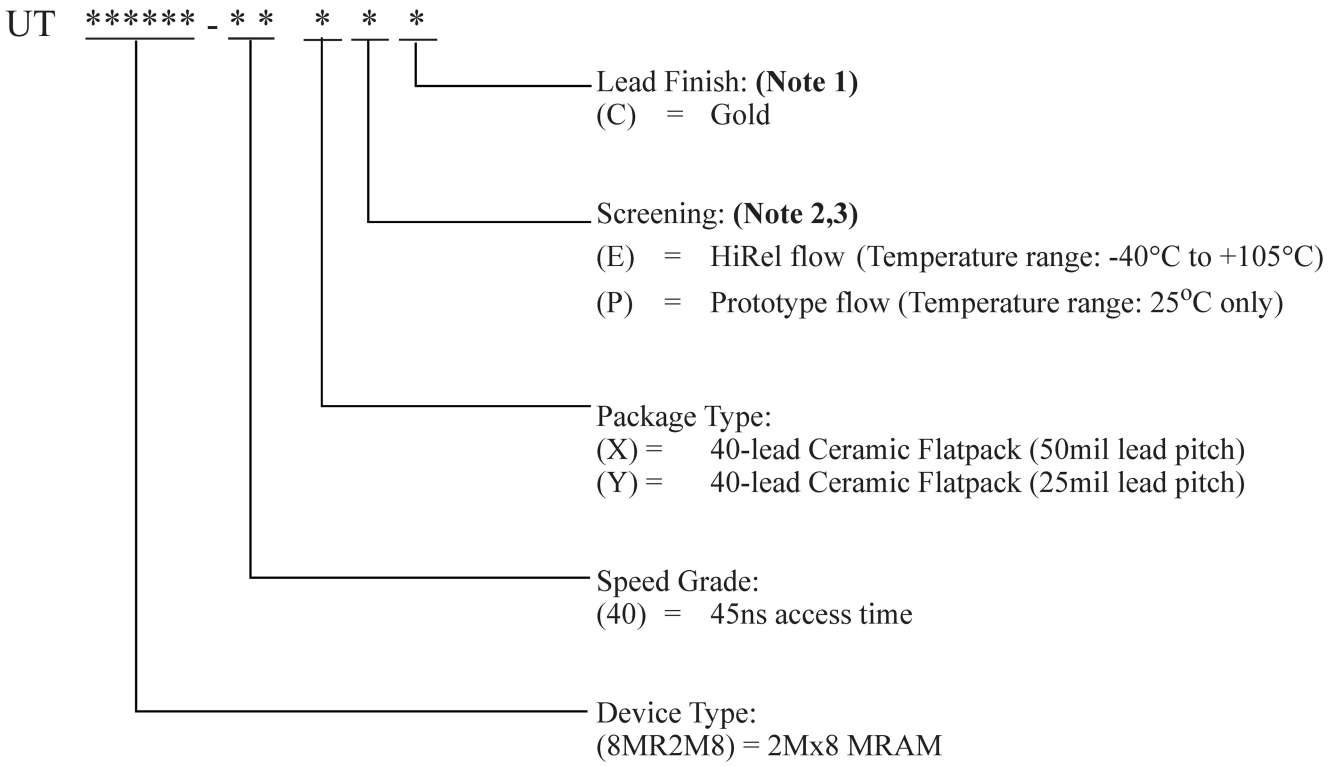
1) Lid is connected to VSS
2) Units are in inches

16Megabit Non-Volatile MRAM

UT8MR2M8

Ordering Information

2M x 8 MRAM:



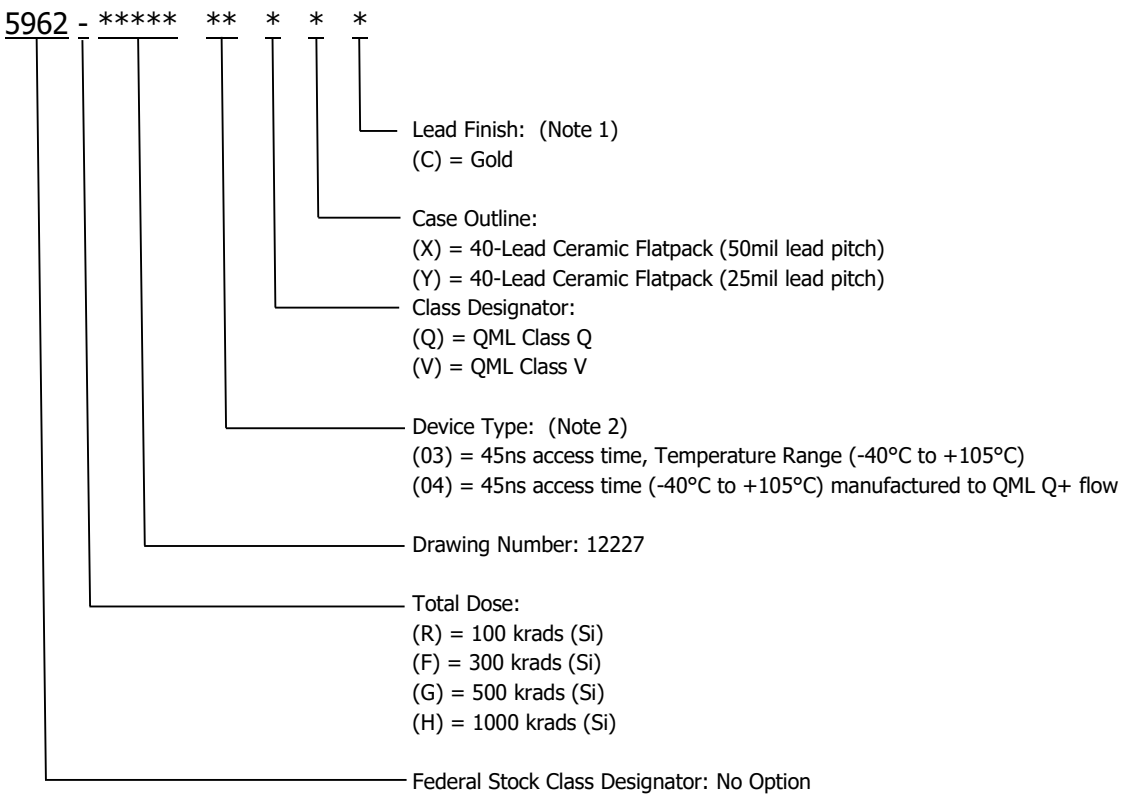
Notes:

1) Lead finish is "C" (Gold) only.
2) Prototype flow per CAES Manufacturing Flows Document. Radiation neither tested nor guaranteed.
3) HiRel flow per CAES Manufacturing Flows Document. Radiation neither tested nor guaranteed.

16Megabit Non-Volatile MRAM

UT8MR2M8

2M x 8 MRAM: SMD



Notes:

1) Lead finish is "C" (Gold) only.
2) CAES Q+ flow, as defined in Section 4.2.2d of SMD, provides QML-Q product through the SMD that is manufactured with CAES standard QML-V flow.

Data Sheet Revision History

Revision Date	Description Of Change	Page(S)
3/15/12	Initial Release of Preliminary Datasheet	All
8/6/12	Changed Temperature Range, Added ECC verbiage, Added Sleep Mode, Updated AC Timing Specifications, Updated Ordering Information	1, 3,6,9, 10,14
9/18/12	Updated AC Timing Specifications, Updated Sleep Mode AC Specifications	8,9,11
12/11/12	Update TID Specification, editorial edits	1,3,All
4/5/13	Changed Sleep Mode to Sleep/Reset Mode and added associated verbiage	2,3,6,11
8/23/13	Updated Power Up and Power Down Sequencing Diagram, Updated Maximum magnetic field during write specification, changed write access time and associated AC timing specifications,	1,4,5,7,9, 10
12/16/13	Final Release of Datasheet, changed read access time and associated AC timing specifications, added temperature range to endurance and retention specification, updated Absolute Maximum Ratings table, updated IDDR and QIZZ specifications, added capacitance specifications, updated Sleep/Reset Mode AC timing specifications, updated package drawings, added revision history	1,5,6,7,11, 12,13,14, 15
4/21/14	Updated supply current specifications. Updated package drawings to reflect different lead length. Format edits.	6, 2,13
9/30/14	Added frequency conditions for I_{DDR} and I_{DDW}	6
January 2016	Added new CAES datasheet template, QML V Achieved, added ZZ/RST description of internal pull-down, updated maximum junction temperature to 150C	All
November 2017	Removed (T) Prototype flow (Temperature range: -40 to +105C) as an ordering option.	14
Sept 2019	Marked QML V from page 1 features list as pending. Added "and remain high during tZZL to note 1 on page 11. Replaced device type 01 and 02 with 03 and 04 and noted QML V option on page 15 "pending contact factory". Added note 3. to page 7 for tGLQV clarification. Previous note 3 is now 4. Moved parenthesis on the first line of intro to be (formerly CAES)	1, 11, 15
Dec 2020	Removed note from page 1 and page 14 that QML V pending, replaced the word aeroflex with Cobham in body of document. Changed PD from 4W to 9W in abs max table, also changed note 3 for abs max table to more common PD= Tjmax-Tcmax/theta JC, added note with ECC-ON always enabled to all DC and AC char tables.	1, 5-10, 14

16Megabit Non-Volatile MRAM

UT8MR2M8

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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