AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PRODUCT CHANGE NOTICE

CAES

1. TITLE	2. DOCUMENT NUMBER
MICROCIRCUIT, DIGITAL, CMOS, SERIAL MICROCODED MULTI-MODE INTELLIGENT TERMINAL AND TRANSCEIVER, SILICON	SPO-2012-PCN-0005
	3. DATE *(Year, Month, Date)*: 2012 Mar 16
4. MANUFACTURER NAME AND ADDRESS: CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME: Tony Sims 6. MANUFACTURER POINT OF CONTACT TELEPHONE: 719-594-8446 7. MANUFACTURER POINT OF CONTACT EMAIL: Tony.Sims@cobhamaes.com

8. CAGE CODE	9. EFFECTIVE DATE	10. PRODUCT IDENTIFICATION CODE	11. BASE PART
65342	1999 APRIL 12	MM019	UT69151XTE5
12. BLANK		13. SMD NUMBER: 5962-94758	14. DEVICE TYPE DESIGNATOR: 08
		15. RHA LEVELS: N/A	16. QML LEVEL: Q
		17. NON QML LEVEL: P & C	18. BLANK

19. PRODUCT CHANGE

The following contended parameters have changed:

Description	Parameter	Old Spec Value	New Spec Value
Write pulse width (contended)	t_{WP2}	1700ns	2060ns
RDY# low time (contended)	t_{RDYL2}	1700ns	2040ns

The parameters identified above apply to each of the following categories as listed in TABLE I of the SMD:

- **Non-multiplexed memory/register write (8-bit), sheet 9**
- **Non-multiplexed memory/register read (8-bit), sheet 9**
- **Non-multiplexed memory/register write (16-bit), sheet 10**
- **Non-multiplexed memory/register read (16-bit), sheet 10**
- **Multiplexed memory/register write (8-bit), sheet 11**
- **Multiplexed memory/register read (8-bit), sheet 11**
- **Multiplexed memory/register write (16-bit), sheet 12**
- **Multiplexed memory/register read (16-bit), sheet 13**

The reason for this change is that CAES identified a worst-case contended memory access scenario where the above parameters can stretch beyond the former specification limit by approximately 300ns.

The worst case contended memory scenario occurs under two modes of device operation: Bus Controller and Monitor.

During the Bus Controller operating mode, a coincident host generated memory access request contends with the device's internally generated memory access request to perform a COMMAND BLOCK READ or COMMAND BLOCK with INTERRUPT INFORMATION UPDATE results in the worst case contended situation. The internally generated access of 8 memory locations will take priority and complete its accesses before the host access is allowed to complete.

Similarly, for the MONITOR operating mode, a worst case COMMAND BLOCK with INTERRUPT INFORMATION UPDATE will holdoff a contended host access in order to complete a burst write of 9 internal memory locations.

The rate of occurrence for a worst case contended memory access is very low due to the sporatic and asynchronous nature of these contended scenarios. Because most systems use the RDY# signal from the UT69151XTE5 to insert wait states to the host processor, successful memory accesses are ensured, regardless of the actual timing of the t_{WP2} and t_{RDYL2} parameters.

20. DISPOSITIONARY RECOMMENDATION:	USE AS IS ☐	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CHECK & USE AS IS ☒

21. ADEPT REPRESENTATIVE	22. SIGNATURE	23. DATE
Timothy L. Meade	Timothy L Meade	**2012, May, 07**