FRONTGRADE

APPLICATION NOTE

UT8SD4MQ2G72

VTT Recommendations

2/3/2025

Version #: 0.0.1

Product Name	Manufacturer Part Number	SMD#	Device Type
18GB DDR4 Memory	UT8SD4MQ2G72	N/A	N/A

Overview

Voltage Termination (VTT) is a critical element in DDR4 memory systems, ensuring signal integrity and proper operation of the memory interface. This application note provides an overview of VTT requirements, design considerations, and implementation strategies for DDR4 memory subsystems.

Introduction

DDR4 memory systems rely on differential signaling and tightly controlled impedance to achieve high-speed operation. The VTT rail is used to terminate signals on the Address/Command/Control (ACC) bus to ensure proper signal levels and prevent reflections. Proper design and implementation of the VTT system are essential for maintaining signal integrity and achieving optimal memory performance.

VTT Requirements for DDR4

1. **Voltage Level**:

   The VTT voltage is defined as VDDQ/2, where VDDQ is the memory IO supply voltage. For DDR4 systems operating at 1.2 V VDDQ, the VTT level is typically 0.6V to 0.675V. Tight tolerance is required, typically within ±3% of the nominal value, to ensure compatibility with the memory and the memory controller. The Vtt supply must track VddQ closely to maintain proper signal integrity. However, since Vtt can be noisy due to the nature of signal termination, it's advised to have a separate power rail for Vtt to prevent noise from affecting the Vdd rail. Adding adequate decoupling capacitors and ensuring low impedance paths are essential for Vtt stability.

   Vdd (Core Supply Voltage): This is the primary power supply for the DRAM core. It needs to be stable and noise-free to ensure reliable operation. It's crucial to maintain this voltage within the specified tolerance, so using high-quality capacitors and proper power filtering is recommended to minimize noise and voltage ripple.

2. **Current Handling**:

   The VTT rail must source and sink current, as the termination resistors are connected to it. For the 18GB DDR4, it is recommended 500mA to 1A. Make sure your power supply design can handle the peak current demand, especially during high-speed data transfers.

3. **Power Isolation**:

   To avoid coupling noise between Vdd and Vtt, separate power planes or isolated power supply paths are strongly recommended. This ensures that noise from the termination voltage (Vtt) does not interfere with the core voltage (Vdd), which could degrade performance or cause errors.

4. **Transient Response**:

   DDR4 memory operates at high frequencies, requiring the VTT rail to respond quickly to load changes. A low-output impedance and adequate decoupling are necessary to minimize voltage deviations during transients.

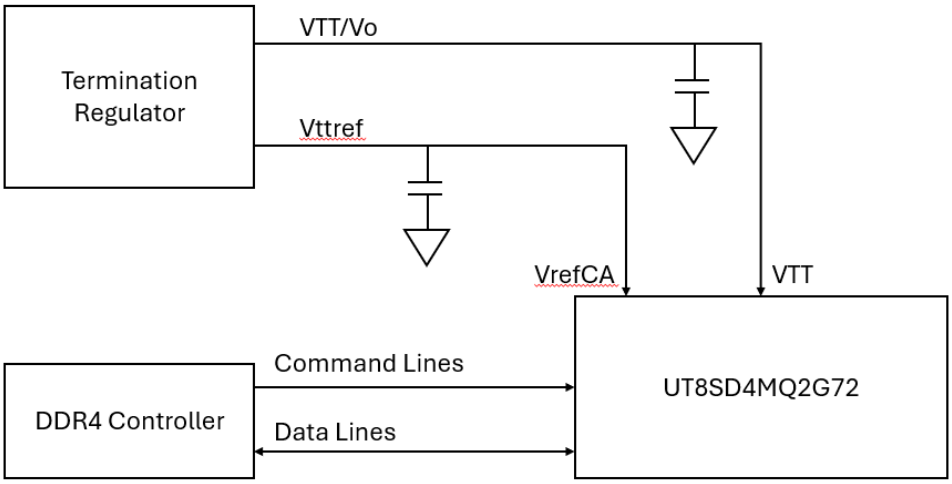
It needs to be stable and noise-free to ensure reliable operation. It's crucial to maintain this voltage within the specified tolerance, so using high-quality capacitors and proper power filtering is recommended to minimize noise and voltage ripple

VTT Design Considerations

VTT Regulator Selection:

- Use a linear regulator or low-dropout (LDO) regulator with the capability to source and sink current. Radiation hardened DDR4 VTT regulators are available from TI (TPS7H3301) and Renesas (ISL70005SEH and ISL73005SEH). Note: TI part has both VTT/Vo and Vttref output. The Renesas part will require an extra LDO for Vttref.
- Key parameters to consider include:
  - Output voltage accuracy.
  - Load regulation.
  - Stability with external capacitors.
  - Thermal performance.

Typical Application Diagram



Conclusion

Designing a reliable VTT system is a critical aspect of DDR4 memory subsystems. By adhering to the guidelines presented in this application note, engineers can ensure robust and efficient operation of their DDR4-based designs.